A Pipelined FSBM Hardware Architecture for
HTDV-H.26x

H. Loukil, A. Ben Atitallah, F. Ghozzi, M. A. Ben Ayed, N. Masmoudi

Abstract—In MPEG and H.26x standards, to eliminate the
temporal redundancy we use motion estimation. Given that the
motion estimation stage is very complex in terms of computational
effort, a hardware implementation on a re-configurable circuit is
crucial for the requirements of different real time multimedia
applications. In this paper, we present hardware architecture for
motion estimation based on "Full Search Block Matching" (FSBM)
algorithm. This architecture presents minimum latency, maximum
throughput, full utilization of hardware resources such as embedded
memory blocks, and combining both pipelining and parallel
processing techniques. Our design is described in VHDL language,
verified by simulation and implemented in a Stratix II
EP2S130F1020C4 FPGA circuit. The experiment result show that the
verified by simulation and implemented in a Stratix II
EP2S130F1020C4 FPGA circuit. The experiment result show that the
optimum operating clock frequency of the proposed design is 89MHz
which achieves 160M pixels/sec.

Keywords—SAD, FSBM, Hardware Implementation, FPGA.

I. INTRODUCTION

In the last few years, video coding systems have been
assuming an increasingly important role in several
application areas tied in with digital television, video-phone
and video-conference, video-surveillance and with the storage
of video data. Several video compression standards have been
established for these different application [1], exploiting both
spatial and temporal redundancies of video sequence to
achieve the required compression rates. Among these
technique, motion estimation has proved to be a fundamental
technique to improve inter-frame prediction in video coding.

It is often the case that video frames that are close in time are
also similar. Therefore, when coding a video frame, it would be
judicious to make as much use as possible of the
information presented in a previously coded frame. One
approach to achieve this goal is to simply consider the
difference between the current frame and a previous reference
frame, as shown in Fig. 1, and code the difference or residual.

When the two frames are very similar, the difference will be
much more efficient to code than coding the original frame. In
this case, the previous frame is used as an estimate of the
current frame. A more sophisticated approach to increase
coding efficiency is to work at the macroblock (NxN pixels)
level in the current frame, instead of processing the whole
frame all at once as described above.

The process is called motion compensated prediction, and
is based on the assumption that most of the motion that the
macroblocks (MB) undergo between frames is a translational
motion. This approach attempts to find, for each NxN
luminance block of a MB in the current frame, the best
matching block in the previous frame. A search window is
usually defined and bounds the area within which the encoder
can perform the search for the best matching block. The
motion of a MB is represented by a motion vector that has two
components; the first indicating horizontal displacement, and
the second indicating vertical displacement. Different criteria
could be used to measure the closeness of two blocks [2]. The
most popular measure is the Sum of Absolute Differences
(SAD) [3], [4] defined by “(1)”.

\[
SAD = \sum_{i=0}^{15} \sum_{j=0}^{15} |Y_{k,l}(i,j) - Y_{k-u,l-v}(i,j)|
\]

(1)

Where \( Y_{k,l}(i,j) \) represents the \((i,j)th\) pixel of a 16 x 16
MB from the current picture at the spatial location \((i,j)\) and
\( Y_{k-u,l-v}(i,j) \) represents the \((i,j)th\) pixel of a candidate MB
from a reference picture at the spatial location \((k,l)\) displaced
by the vector \((u,v)\).

To find the MB producing the minimum mismatch error, we
need to compute SAD at several locations within a search
window. This approach is called full search or exhaustive
search, and is usually computationally expensive, but on the
other hand yields good matching results. To perform FSBM
algorithm, we must execute \((2p+1)^2\) SAD functions. As we
see that FSBM algorithm is very complex in term of
computation, which can be a significant problem in a real time
termed video coding using software solution [5], [6]. There are
several block-matching algorithms (BMAs) [7]-[9] that can be
used for motion estimation but the FSBM algorithm is preferred due to their relative simplicity, low-control overhead and achieves optimal performances in terms of PSNR (Peak Signal to Noise Ratio) for a given compression factor. Nowadays configurable Field Programmable Gate Array (FPGA) technology is able to execute complex embedded video processing in real time. Thus, to reduce complexity and to take advantage of the FSBM algorithm a pipelined hardware implementation in FPGA of this algorithm is proposed. In our study, we suppose that MB size is 16x16 and search area is 32x32 pixels wide. Therefore, around current MB in current frame, we insert 8 pixels (p=8). Generally, current MB and search area have an N×N an (N+2p)×(N+2p) pixel-size respectively as shown in Fig. 2.

Fig. 2 The current MB position in the search area

This paper is organized as follows. Section 2 presents different hardware architectures for FSBM. Section 3 describes our proposed hardware architecture for FSBM algorithm. The simulation and synthesis results for all architectures are presented and discussed in section 4. Finally, section 5 concludes the paper.

II. DIFFERENT ARCHITECTURE FOR FSBM

In literature, different architectures are proposed to implement the FSBM algorithm [11]-[16], but these architectures have in important clock cycles number to compute the motion vector. This high number of clock makes these architectures unsuited to achieve for example the processing requirements of high definition TV (HDTV 1080i, 1920x1088@60Hz) which requires 125M pixels/sec. This section presents briefly these different architectures and our pipelined hardware architecture.

A. T. Komarek and P. Pirsch Architecture

All figures in this section are represented for N=3 and p=2. All architectures in this section are composed by 4 components:

- AD: calculate the Absolute difference value between tow pixels and accumulate present value with previous value.
- R: Registers allows the data synchronization
- A: Accumulator.
- M: Comparator.

1) AB1 Architecture

Fig. 3 represents AB1 architecture. It’s composed by N “AD”, (2N+1) registers, one accumulator and one comparator. For calculate different SAD’s (N=16 and p=8), we use 16 ADs, 33 registers, one accumulator and one comparator. Each AD has one input for MB and an others input for search window. To calculate (2p+1)^2 SAD’s we use 9250 clock cycles. The detail of intermediate operation of this architecture is described in [11].

2) AB2 Architecture

Fig. 4 represent AB2 architecture. It’s composed by N×N “AD”, (N×N+(N-1)×N+2N+1) registers, N accumulators and one comparator.

For N=16 and p=8, we use 256 ADs, 529 registers, 16 accumulator and one comparator for calculate (2p+1)^2 SAD’s. Each AD have one input for search window. The interesting point in this architecture is the storage of MB pixels in Each AD. With this idea, for calculate all SAD’s and the motion vector, we use 579 clock cycles. The detail of intermediate operation of this architecture is described in [11].

3) AS1 Architecture

Fig. 5 represents AS1 architecture. It’s composed by Ψ “AD” (Ψ is equal to number of displacement in search window), (3×(Ψ-1)+3×Ψ+1) registers, (Ψ) accumulators and (Ψ+1) comparator. For N=16 and p=8, we use 17 ADs, 100 registers, 17 accumulators and 18 comparators. For all ADs, we have on input for MB and other input for search window. The detail of intermediate operation of this
architecture is described in [11]. For calculate all SAD’s and the motion vector, we use 8722 clock cycles.

4) Architecture AS2

Fig. 6 represents AS2 architecture. It’s composed by $N\times \Psi \cdot \text{AD}$, $3x(\Psi)\times N-1 + Nx(\Psi-1)+ 3x\Psi + 1+c$ registers, $\Psi$ accumulators and $\Psi+1$ comparators. ($c = \Psi-(\Psi-1)+\Psi-(\Psi-2)+...+(\Psi-2)$).

For this architecture we use 272 Ads, 685 registers, 17 accumulators and 18 comparators ($N=16$ and $p=8$). Each AD has one input for MB and an others input for search window. To calculate $(2p+1)^2$ SAD’s we use 577 clock cycles. The detail of intermediate operation of this architecture is described in [11].

B. K. M. Yang and al. Architecture

This architecture is composed by $N$ PEs, $(N-1)$ flip-flop, $N$ multiplexers (MUX) and one comparator for compute the minimum SAD and the motion vector. All this components is presents in fig. 7.

For $N=16$ and $p=8$, we use 16 PEs, 15 DFF and 16 MUX. The intermediate operation of each PE and synchronization of data are presented in [12]. For calculate all SAD’s and the motion vector, we use 4370 clock cycles.

C. H. Hsieh and al. Architecture

This architecture is composed by $(N\times N)$ processor element (PE), $(N\times P)$ Shift register (SR), Parallel Adder and comparator. Fig. 8 presents the connection between these elements.

For $N=16$ and $P=8$, we use 256 PEs, 128 SRs, one Parallel Adder and one comparator. We use 1028 clock cycles for calculate $(2p+1)^2$ SAD’s and the motion vector. You can find all detail of this architecture in [13].

D. H. Yeo and al. Architecture

This architecture is present in fig. 9. It is composed by $N\times N$ PEs, 2 MUX, one input for MB and tow input for search window. In [14], you can find the intermediate operation of this architecture. For $N=16$ and $P=8$, we use 256 PEs and 2 MUX. The motion vector is outputted after 547clock cycles.

F. M. Yang and al. Architecture

In this architecture, you can find $N\times N$ PEs, N MUX, input for MB and tow input for search window, $(N+1)$ comparator for obtained the motion vector. Therefore, for synchronization of data, we use $N$ registers for MB and $(2\times N)$ registers for search window. Fig. 10 present the schematic of this architecture. In this architecture “C” is input for MB and $(P,P’)$ is input for search window. All detail for this...
architecture is presented in [15]. For \( N=16 \) and \( P=8 \), we use 256 PEs, 16 MUX and 48 registers. For calculate all SAD's and the motion vector, we use 534 clock cycles.

E. Y. S. Jehng and al. Architecture

Fig. 11 present the diagram of this architecture for \( N=4 \). It's composed by \( N \times N \) “D” for computing the absolute value, \((N \times N -1)\) accumulator and one comparator. In addition, we find \( N \times N \) input for MB and \( N \times N \) input for search window. In [16], you can find the intermediate operation of this architecture.

For calculate all SAD’s and the motion vector for \( N=16 \) and \( P=8 \), we use 256 “D”, 255 accumulator and one comparator. The motion vector is outputted after 290 clock cycles.

### III. PROPOSED ARCHITECTURE

#### A. Proposed structure

In order to realize FSBM algorithm, various architectures have been proposed. By examining these architectures, we conclude that processing elements (PEs), address generator and data memories are indispensible and necessary components for FSBM algorithm implementation. In fact, PE accomplishes the computation of block distortion measure (SAD). Address generator generates the address to memories and transfer data from each memory block to the corresponding processing elements. Consequently, the proposed FSBM architecture is illustrated in Fig. 12. Our proposed architecture is composed of multiplexed registers, memories, Flip-flops, absolute difference components, accumulators, and a comparator for selecting the minimum SAD provided by each PE. Controller module contains the address generator engine that produces the memory addresses and transfers data from each memory block to the corresponding PEs.

#### B. Data memories control

For this architecture, we need a combination of 12 single-port memories that enables the reading of 12 pixels for every clock cycle (8 memories for the search area and 4 memories for the current MB). Each memory is generated by LPM mega-functions library in order to take advantage of the “StratixII” embedded RAM blocks. We must read pixels from input frames by using VHDL description with various “TEXTIO” instructions (camera entity) and store them in 12 memories. Then, the data coming from camera entity must be organized on these memories as shown in Table 1 and Table 2.

Table 1 shows that we have stored search area pixels in 8 separate memories in order to address 8 pixels at each clock cycle. These memories are presented by the search area memory block in the proposed architecture.

Table 2 shows that we have stored pixels of current MB in 4 memories in order to address 4 data’s at each clock cycle. These memories take parts of the current MB memory block in the proposed architecture.

AFTER memorizing search area and current MB, we will compute 289 SADs. That’s why we must respect the memories read order presented in Table 3.

To test and simulate memory blocks, we use a test bench file allowing the mapping of each memory component with another component called “camera”, which allows the reading of the pixels values from PGM frame files. For the search area, we use 8 memories of 128 bytes each. In fact, the search area has 32x32 pixels size and 25x25=210=1024 addresses. Each address consist of 8 bits data, thus we obtain 1024 bytes. For the current MB, we use 4 memories of 64 bytes each. Indeed, the size of a current MB is 16x16 pixels requiring 24x24 =28=256 addresses. Each address consists of 8 bits data, thus we obtain 256 bytes. Memories are synchronous and they can be used in writing or reading mode. In writing mode, the memories receive frame files data and store each one in the specified address.

#### C. Multiplexers block diagram

Multiplexers are used to select the data search area, and to allow horizontal movement for the execution of 17 SADs in parallel. Fig. 13 depicts the multiplexer’s block.
Fig. 13 Block of the multiplexers

F1 to F8 represent the pixels generated by the various memories of the search area and will be organized 2 by 2. This block consists of 16 multiplexers as shown in fig. 13. S1 to S16 represent the outputs of multiplexers, and correspond to the 16 horizontal movements (in the first horizontal movement we don’t use any multiplexer). The Flip-Flop block allows during the processing of 289 SADs to read the different memories only one time and pass various data to each PE in order to compute the corresponding SAD.

D. SAD calculation

Processing elements block represented in fig. 12 is composed by 1156 inputs for the search area data (X) and 1156 inputs for the current MB data (Y). This block allows the computation of 289 SADs in a mixed mode: parallel and pipeline. It is possible to combine 4 processors elements (PE) in one engine in order to compute SAD 16x16 as shown on fig. 14.

Each PEi allows the computation of a SAD 16x4. The parallel adder performs the sum of 4 SADs 16x4 values for a given SAD 16x16. That’s why we dispose of 1156 inputs (4*289) for both search area and current MB. Since we use 4 PEs to compute 289 SADs. Fig. 15 represents the internal structure of each PE. Our proposed algorithm allows the computation of 16x16 SAD in 64 cycles instead of 256 cycles for the existing architectures. Table 4 represents the necessary method for computing 289 SADs in mixed mode: parallel and pipeline.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

In the previous section, we present an overview of all architecture. These architectures are described with VHDL language. Result of synthesis on the “STRATIXII family – EP2S130F1020C4” component is presented in the following table:

<table>
<thead>
<tr>
<th>Resources</th>
<th>Avail</th>
<th>Used</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input/output</td>
<td>743</td>
<td>76</td>
<td>10%</td>
</tr>
<tr>
<td>Logic ports</td>
<td>106032</td>
<td>7004</td>
<td>66%</td>
</tr>
<tr>
<td>Memory Bits</td>
<td>6747840</td>
<td>10240</td>
<td>&lt;1%</td>
</tr>
</tbody>
</table>

The maximum clock frequency is 89 MHz. The experimental results show that just 140 cycles is necessary to compute the final motion vector. With this result, we can execute 160M pixels/sec which is suited to process HTDV (1920x1088@60Hz) video sequences. The table 6 and 7 resumes the functional parameter and synthesis results for all presented architectures respectively. Form these tables, our pipelined FPGA architecture takes the minimum execution time for compute the motion vector.

V. CONCLUSION

In this paper, we have proposed the motion estimation architecture. Our pipelined architecture benefits from several PE engines executing in parallel and pipeline mode. This will solve the real time constraint and enable a better efficiency in HTDV video coding. It has been proved through our study that FPGA is an ultimate solution for the design of a motion estimation algorithm based on FSBM conception through the hardware description language (VHDL).

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REFERENCES


### TABLE I

**DATA MEMORIES STRUCTURE FOR SEARCH AREA**

<table>
<thead>
<tr>
<th>Memory F1</th>
<th>Memory F2</th>
<th>Memory F3</th>
<th>Memory F4</th>
<th>Memory F5</th>
<th>Memory F6</th>
<th>Memory F7</th>
<th>Memory F8</th>
</tr>
</thead>
<tbody>
<tr>
<td>F(0,0)</td>
<td>F(1,0)</td>
<td>F(2,0)</td>
<td>F(3,0)</td>
<td>F(16,0)</td>
<td>F(17,0)</td>
<td>F(18,0)</td>
<td>F(19,0)</td>
</tr>
<tr>
<td>F(4,0)</td>
<td>F(5,0)</td>
<td>F(6,0)</td>
<td>F(7,0)</td>
<td>F(20,0)</td>
<td>F(21,0)</td>
<td>F(22,0)</td>
<td>F(23,0)</td>
</tr>
<tr>
<td>F(8,0)</td>
<td>F(9,0)</td>
<td>F(10,0)</td>
<td>F(11,0)</td>
<td>F(24,0)</td>
<td>F(25,0)</td>
<td>F(26,0)</td>
<td>F(27,0)</td>
</tr>
<tr>
<td>F(12,0)</td>
<td>F(13,0)</td>
<td>F(14,0)</td>
<td>F(15,0)</td>
<td>F(28,0)</td>
<td>F(29,0)</td>
<td>F(30,0)</td>
<td>F(31,0)</td>
</tr>
<tr>
<td>F(0,1)</td>
<td>F(1,1)</td>
<td>F(2,1)</td>
<td>F(3,1)</td>
<td>F(16,1)</td>
<td>F(17,1)</td>
<td>F(18,1)</td>
<td>F(19,1)</td>
</tr>
<tr>
<td>F(0,2)</td>
<td>F(1,2)</td>
<td>F(2,2)</td>
<td>F(3,2)</td>
<td>F(16,2)</td>
<td>F(17,2)</td>
<td>F(18,2)</td>
<td>F(19,2)</td>
</tr>
<tr>
<td>F(12,1)</td>
<td>F(13,1)</td>
<td>F(14,1)</td>
<td>F(15,1)</td>
<td>F(28,1)</td>
<td>F(29,1)</td>
<td>F(30,1)</td>
<td>F(31,1)</td>
</tr>
<tr>
<td>F(12,2)</td>
<td>F(13,2)</td>
<td>F(14,2)</td>
<td>F(15,2)</td>
<td>F(28,2)</td>
<td>F(29,2)</td>
<td>F(30,2)</td>
<td>F(31,2)</td>
</tr>
</tbody>
</table>
TABLE IV
ARCHITECTURE OPERATION

<table>
<thead>
<tr>
<th>Clock cycle</th>
<th>SAD0</th>
<th>SAD1</th>
<th>SAD2</th>
<th>SAD3</th>
<th>SAD4</th>
<th>SAD287</th>
<th>SAD288</th>
</tr>
</thead>
<tbody>
<tr>
<td>1+(4*0)</td>
<td>R(0,0)-F(0,0)</td>
<td>R(1,0)-F(1,0)</td>
<td>R(2,0)-F(2,0)</td>
<td>R(3,0)-F(3,0)</td>
<td>R(0,0)-F(0,0)</td>
<td>R(1,0)-F(1,0)</td>
<td>R(2,0)-F(2,0)</td>
</tr>
<tr>
<td>2+(4*0)</td>
<td>R(4,0)-F(4,0)</td>
<td>R(5,0)-F(5,0)</td>
<td>R(6,0)-F(6,0)</td>
<td>R(7,0)-F(7,0)</td>
<td>R(4,0)-F(4,0)</td>
<td>R(5,0)-F(5,0)</td>
<td>R(6,0)-F(6,0)</td>
</tr>
<tr>
<td>3+(4*0)</td>
<td>R(8,0)-F(8,0)</td>
<td>R(9,0)-F(9,0)</td>
<td>R(10,0)-F(10,0)</td>
<td>R(11,0)-F(11,0)</td>
<td>R(8,0)-F(8,0)</td>
<td>R(9,0)-F(9,0)</td>
<td>R(10,0)-F(10,0)</td>
</tr>
<tr>
<td>4+(4*0)</td>
<td>R(12,0)-F(12,0)</td>
<td>R(13,0)-F(13,0)</td>
<td>R(14,0)-F(14,0)</td>
<td>R(15,0)-F(15,0)</td>
<td>R(12,0)-F(12,0)</td>
<td>R(13,0)-F(13,0)</td>
<td>R(14,0)-F(14,0)</td>
</tr>
<tr>
<td>1+(4*1)</td>
<td>R(0,1)-F(1,1)</td>
<td>R(1,1)-F(2,1)</td>
<td>R(2,1)-F(3,1)</td>
<td>R(3,1)-F(4,1)</td>
<td>R(0,1)-F(1,1)</td>
<td>R(1,1)-F(2,1)</td>
<td>R(2,1)-F(3,1)</td>
</tr>
<tr>
<td>2+(4*1)</td>
<td>R(4,1)-F(4,1)</td>
<td>R(5,1)-F(5,1)</td>
<td>R(6,1)-F(6,1)</td>
<td>R(7,1)-F(7,1)</td>
<td>R(4,1)-F(4,1)</td>
<td>R(5,1)-F(5,1)</td>
<td>R(6,1)-F(6,1)</td>
</tr>
<tr>
<td>1+(4*2)</td>
<td>R(0,2)-F(0,2)</td>
<td>R(1,2)-F(1,2)</td>
<td>R(2,2)-F(2,2)</td>
<td>R(3,2)-F(3,2)</td>
<td>R(0,2)-F(0,2)</td>
<td>R(1,2)-F(1,2)</td>
<td>R(2,2)-F(2,2)</td>
</tr>
<tr>
<td>2+(4*2)</td>
<td>R(4,2)-F(4,2)</td>
<td>R(5,2)-F(5,2)</td>
<td>R(6,2)-F(6,2)</td>
<td>R(7,2)-F(7,2)</td>
<td>R(4,2)-F(4,2)</td>
<td>R(5,2)-F(5,2)</td>
<td>R(6,2)-F(6,2)</td>
</tr>
<tr>
<td>1+(4*16)</td>
<td>R(0,16)-F(0,16)</td>
<td>R(1,16)-F(1,16)</td>
<td>R(2,16)-F(2,16)</td>
<td>R(3,16)-F(3,16)</td>
<td>R(0,16)-F(0,16)</td>
<td>R(1,16)-F(1,16)</td>
<td>R(2,16)-F(2,16)</td>
</tr>
<tr>
<td>1+(4*19)</td>
<td>R(0,0)-F(15,16)</td>
<td>R(0,0)-F(16,16)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## TABLE VI
### FUNCTIONAL RESULTS FOR DIFFERENT ARCHITECTURES

<table>
<thead>
<tr>
<th>N=16 et P=8</th>
<th>AB1</th>
<th>AB2</th>
<th>AS1</th>
<th>AS2</th>
<th>Heish</th>
<th>F. M. Yang</th>
<th>Jehng</th>
<th>Yeo</th>
<th>Proposed Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor element number</td>
<td>16</td>
<td>256</td>
<td>17</td>
<td>272</td>
<td>256</td>
<td>17</td>
<td>289</td>
<td>512</td>
<td>289</td>
</tr>
<tr>
<td>Architecture topology</td>
<td>1-D</td>
<td>2-D</td>
<td>1-D</td>
<td>2-D</td>
<td>1-D</td>
<td>2-D</td>
<td>2-D</td>
<td>2-D</td>
<td>2-D</td>
</tr>
<tr>
<td>Input port number for search window</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>1</td>
<td>2</td>
<td>256</td>
<td>2</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Input port number for MB</td>
<td>16</td>
<td>1</td>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Clock cycles number for compute the motion vector</td>
<td>9250</td>
<td>579</td>
<td>8722</td>
<td>577</td>
<td>1028</td>
<td>4370</td>
<td>534</td>
<td>290</td>
<td>547</td>
</tr>
</tbody>
</table>

## TABLE VII
### SYNTHESIS RESULTS FOR ALL ARCHITECTURES

<table>
<thead>
<tr>
<th>N=16 et P=8</th>
<th>AB1</th>
<th>AB2</th>
<th>AS1</th>
<th>AS2</th>
<th>Heish</th>
<th>K. M. Yang</th>
<th>F. M. Yang</th>
<th>Jehng</th>
<th>Yeo</th>
<th>Proposed Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic element number</td>
<td>5153</td>
<td>17179</td>
<td>2068</td>
<td>20548</td>
<td>14010</td>
<td>1654</td>
<td>26799</td>
<td>69917</td>
<td>15866</td>
<td>70004</td>
</tr>
<tr>
<td>Memory bits number</td>
<td>10240</td>
<td>10240</td>
<td>10240</td>
<td>10240</td>
<td>-</td>
<td>10240</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>10240</td>
</tr>
<tr>
<td>Maximum frequency (Mhz)</td>
<td>142.51</td>
<td>115.97</td>
<td>111.17</td>
<td>160.62</td>
<td>128.09</td>
<td>134.86</td>
<td>96.64</td>
<td>50.97</td>
<td>70.01</td>
<td>89</td>
</tr>
<tr>
<td>Latency time</td>
<td>2.6</td>
<td>0.922</td>
<td>2.173</td>
<td>2.593</td>
<td>2.41</td>
<td>0.973</td>
<td>8.844</td>
<td>10.278</td>
<td>8.717</td>
<td>7</td>
</tr>
<tr>
<td>Execution time (ns)</td>
<td>64909.85</td>
<td>4993.639</td>
<td>78456.563</td>
<td>3594.995</td>
<td>8028.006</td>
<td>32404.523</td>
<td>5534.676</td>
<td>5705.878</td>
<td>7399.781</td>
<td>1579.432</td>
</tr>
</tbody>
</table>

Hassen Loukil received electrical engineering degree from the National School of Engineering-Sfax (ENIS) in 2004. His received his MS degree in electronic engineering from the National School of Engineering-Sfax (ENIS) in 2005. He is currently researcher in the Laboratory of Electronics and Information Technology and an assistant at the University of Sfax, Tunisia. His research interests include signal and image processing, hardware implementation using FPGA, embedded systems technology.

Nouri Masmoudi received electrical engineering degree from the Faculty of Sciences and Techniques-Sfax, Tunisia, in 1982, the DEA degree from the National Institute of Applied Sciences-Lyon and University Claude Bernard-Lyon, France in 1982. From 1986 to 1990, he prepared his thesis at the laboratory of Power Electronics (LEP) at the National school Engineering of Sfax (ENIS). He received his PhD degree at the National school Engineering of Tunis (ENIT), Tunisia in 1990. From 1990 to 2000, he was an assistant professor at the electrical engineering department-ENIS. Since 2000, he has been an associate professor and head of the group ‘Circuits and Systems’ in the Laboratory of Electronics and Information Technology. Since 2003, He is responsible for the Electronic Master Program at ENIS. His research activities have been devoted to several topics: design, telecommunication, embedded systems and information technology, Video Coding (Motion Estimation, Mode Decision, Image Interpolation, and Denoising).