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Novel linear autozeroing floating-gate amplifier for ultra low-voltage applications

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Abstract—In this paper we present a linear autozeroing ultra low-voltage amplifier. The autozeroing performed by all ULV circuits is important to reduce the impact of noise and especially avoid power supply noise in mixed signal low-voltage CMOS circuits. The simulated data presented is relevant for a $90nm$ TSMC CMOS process.

Keywords—Low-voltage, transconductance amplifier, linearity, floating-gate.

I. Introduction

The supply voltage in modern CMOS processes is pushed down due to the need for high performance digital circuits. This is due to electrical limitations for deep submicron devices. In addition, the leakage currents in general and the gate tunneling currents in particular will impose significant challenges in circuit design. The electrical challenges that are exposed because of digital applications driven by a need for increased speed are far greater for analog circuit design than for digital applications. A typical lower limit for the supply voltage in analog circuits is determined by the threshold voltage and saturation voltage $V_{DD} > V_t + 2V_{DS-sat}$. In addition, it will be necessary to provide gain and headroom which will push the supply voltage up. By taking advantage of floating-gate transistors the supply voltage can be reduced further. Because of the leakage current we can only use floating-gate transistors if the dc level of the gate voltage is ensured through a resistive network or via a frequent refresh. The circuits presented in this paper are precharged to $V_{DD}/2$ during a recharge and autozeroing phase. The amplifier discussed is dc independent, i.e. it resonds to a change in the input signal and not to the dc level. This is an important feature when the dc level of the external input is not known. The autozeroing function prevents the circuits from drifting to the supply rails.

By using floating gates[1][2][3] we can transfer focus from transistor sizes to capacitor sizes in order to obtain a linear response of amplifiers. The use of input capacitors will however reduce the transconductance and to compensate for this we may use two different differential input stages which increase the transconductance and linearity. The amplifier presented in this paper performs frequent autozeroing which reduces the impact of power supply noise.

In this paper we combine two different ultra low voltage (ULV) differential amplifiers to increase both the transconductance and linearity. In section II the clocked semi-floating-gate (CSFG) transistors are exploited in ultra low-voltage (ULV) analog design. CSFG analog circuits are presented in section III, including a current mirror and a pseudo differential pair. The transconductance amplifier is presented in section IV and the conclusion is given in section V.

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II. CSFG transistors

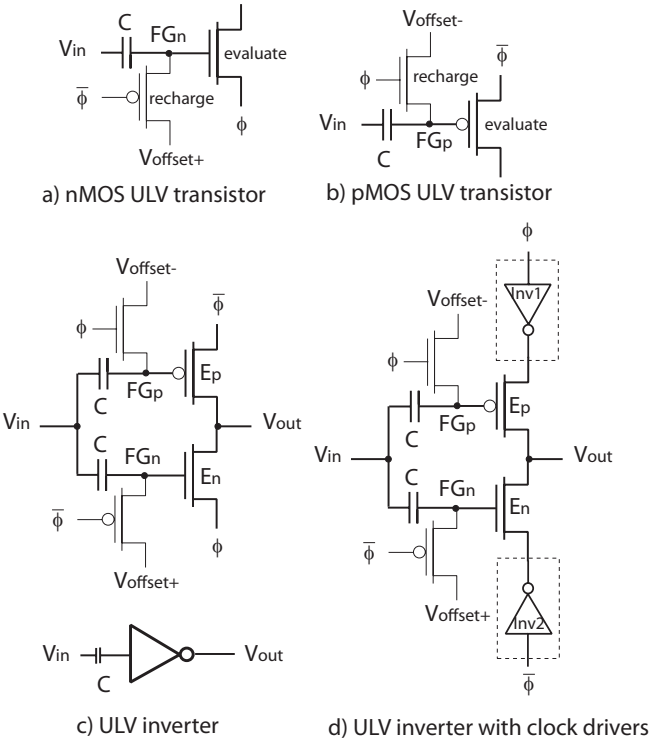

Fig. 1. *nMOS and pMOS clocked semi-floating-gate (CSFG) transistors and ULV inverter with clock drivers.*

The clocked-semi-floating-gate transistors are shown in Fig. 1 a) and b). The recharge transistors are controlled by clock signals which will force the nMOS evaluate transistor gate terminal (FGn) to V_{DD} in the recharge mode, i.e. $\phi = 1$, and the pMOS transistor gate terminal to gnd. Any input transitions will affect the evaluate transistors gate voltages either by a positive or a negative charge. By powering up the gate to source voltages in an initialization phase we are able to reduce the power supply without decreasing the ON current provided by the enhanced transistors. The aim is to maintain a high current level combined with a very low supply voltage. The enhancement can be viewed as an active threshold voltage shift. .

For very low supply voltages the CSFG biasing will not have a significant impact on the current level, and hence neither relative ON nor OFF currents are large. For increasing supply

voltages, up to $V_{DD} = V_t$, the relative current increases. For $V_{DD} \leq 0.65Vt$, assuming that $k_{in} \leq 0.7$, where $k_{in} = C/C_{fg}$ and C_{fg} is the total capacitance seen by the floating gate, the gate to source voltage will never reach the threshold voltage. In this case the transistor will operate in the subthreshold regime. The transistors may operate in strong inversion if the supply voltage is close to or above the threshold voltage of the transistors. Furthermore, dummy recharge transistors may be included to reduce noise induced by the clock signal driving the recharge transistor.

III. CSFG AUTOZEROING ANALOG CIRCUITS

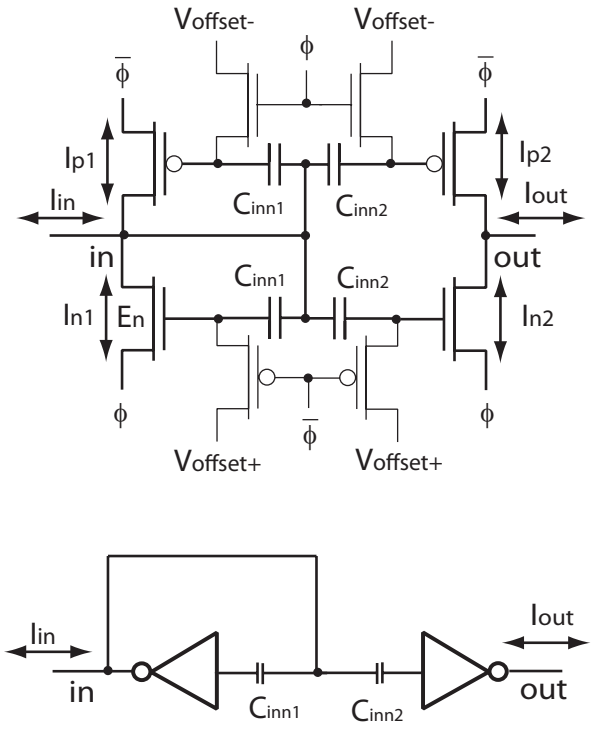

Fig. 2. *Symmetric ULV current mirror.*

In Fig. 2 a symmetric current mirror is shown [4]. The symmetric current mirror can be drawn using the floating-gate inverter symbols. The input current I_{in} will pull the input terminal towards V_{DD} or V_{SS} depending on the polarity of the current. A negative current will pull the input terminal down and a positive input current will pull the input up. The input current will be matched by a current provided by the inverter in the I to V converter. The I to V converter will generate an input voltage to drain the actual input current. If the input current is equal to the recharge current the circuit is stable and the input voltage is equal to $V_{DD}/2$. Any change in the input current will affect the floating gate voltages such that the input current is drained by the inverter in the I to V converter. The drained input current will be available at the output due to a corresponding change in the floating gate of the inverter producing the output current. If the capacitors, C_{inn1} and C_{inn2} or C_{inp1} and C_{inp2}, are equal the voltage change at the semi floating gates and hence the output current will match the current running through the inverter in the I to V converter which is equal to the input current. We have not considered a natural source for the input current and a natural drain or load for the output current. A positive input current will be drained by an equal current running through the nMOS transistor of the inverter in the I to V converter caused by a increase in the voltage of the input terminal. A negative input current will lower the input terminal voltage and the input current will be drained by an increased pMOS transistor current of the I to V converter.

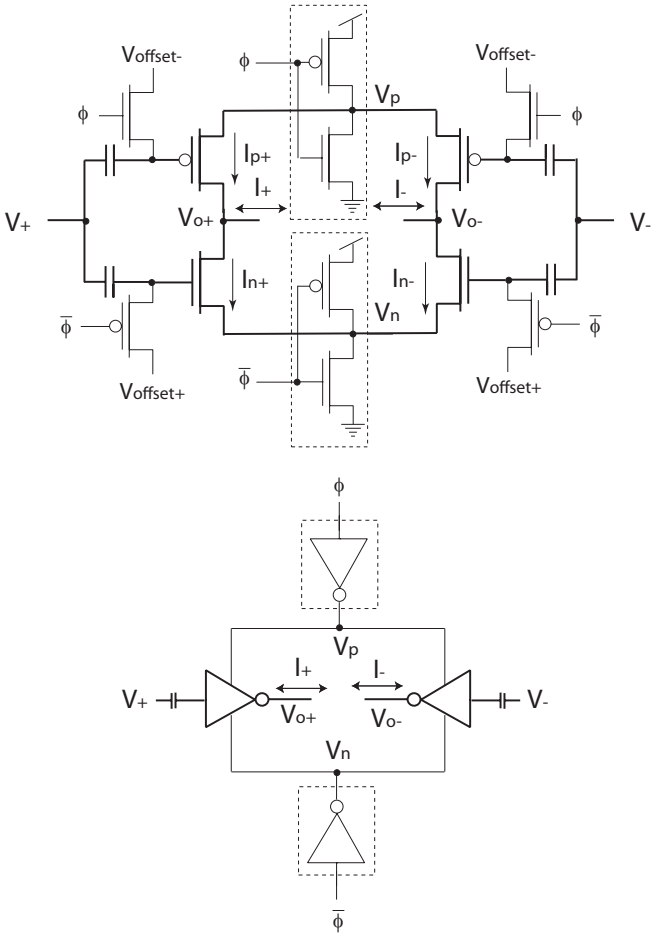

Fig. 3. *Symmetric ULV differential pair.*

A ULV inverter including clock driver inverters is shown in Fig. 1 d). The clock drivers located close to the source/drain terminals of the evaluate transistors En and Ep may be used to provide current sources. The inverters labeled Inv1 and Inv2 may be used as bias transistors in a pseudo differential pair. The effective voltage of the evaluating transistors will be determined by the the supply voltage and the capacitive division associated with the input capacitances. By using the transistors of the clock driver that provide the reference voltage to the circuit we may configure two CSFG transistors in parallel powered by the same clock driver to provide a CSFG pseudo differential pair as shown in Fig. 3 [5]. The clock driver (inverter) provides two alternative current sources dependent on the the clock driver input $\overline{\phi}$. In the

case when $\overline{\phi}$ is 0 the floating-gates will be recharged to V_{DD} and the pMOS transistor of the clock driver will be on and the currents running the evaluate transistors will be in the opposite direction than shown in the figure. The CSFG circuits resembles precharge domino logic characterized by a precharge or recharge phase and an evaluation phase. In the recharge phase the active transistors are recharged by pulling the gate voltage to V_{offset}.

In the recharge mode two tasks needs to be performed. The semi floating-gate FG nodes of the nMOS transistors will be forced to $V_{offset+}$, and pMOS transistors to $V_{offset-}$, through the recharge transistors and the currents running through the evaluate transistors must contribute to the initialization of the output nodes. We may assume that the inputs are recharged to $V_{DD}/2$ and that there will a pMOS CSFG transistor connected to each output and thereby providing a current source connected to gnd. The nMOS bias transistor current is determined by the nMOS transistor of the clock driver, i.e. the gate to source voltage V_{DD} and transistor size. The bias transistor will have a gate to source voltage equal to V_{DD}. Due to the offset imposed on the floating-gates the two transistors of the pseudo differential pair may have a gate to source voltage higher than V_{DD}. In order for the bias transistor to pull the required amount of current running through the pseudo differential pair we increase the width of the bias transistor.

The symmetric ULV pseudo differential pair is shown in Fig. 3. A nMOS diff pair is stacked on top of a pMOS diff pair. When using the symmetric pseudo deifferential pair each input serve as input to an ULV inverter with degenerated supply voltag. In addition, the transconductance is enhanced because any change at the input will cause a change in all components. For example, if $\Delta V_+ > 0$ and $\Delta V_- = 0$, the direct response will be an increase in I_{n+} and a decrease in I_{p+} expressed as $\Delta I_{n+} > 0$ and $\Delta I_{p+} < 0$. The indirect response may be expressed as $\Delta V_n > 0$ and $\Delta V_p > 0$, hence $\Delta I_{n-} < 0$ and $\Delta I_{p-} > 0$. By combining the current components into the output current we obtain $\Delta I_{out} \equiv \Delta I_{n+} + \Delta I_{p+} + \Delta I_{n-} + \Delta I_{p-}$. If we assume that $\Delta I_{n+} = -\Delta I_{p+} = -\Delta I_{n-} = \Delta I_{p-}$ we can express the change in output current as $\Delta I_{out} = 4 \times \Delta I_{n+}$. The increased transconductance is however only valid in the linear region and for small input signals. We may increase the linear region of the differential pair by reducing the transconductance of each transistor. This is easily achieved by decreasing the floating capacitors C_{in}. However, the overall transconductance and gain will then be reduced as well. By adding an additional input stage that provide additional currents which responds to to larger input signals we may increase the linear range without reducing the transconductance.

IV. ULV AMPLIFIER

The ULV transconductance amplier is shown in Fig. 4. The ouput current of the amplifier is provided by two parallel different input stages and two output stages.

There are two different input stages

1) **INV1** and **INV2**. This is a symmetric pseudo differential pair where the bias current is provided by a clock driver transistors operating in saturation and regulating voltages V_n and V_p. The transconductance is determined by the capacitance C_1 relative to the total capacicatnce seen by the floating gates of the INV1 and INV2 inverters. The transconductance can be modelled by $k_1 \times \Delta V_{in}$.
2) **INV4**. The two inputs V_+ and V_- are combined through an analog inverter with gain -1. The output of INV4 can besexpressed as $\Delta V_B = (\Delta V_- - \Delta V_+)/2 = \Delta V_{in}/2$.

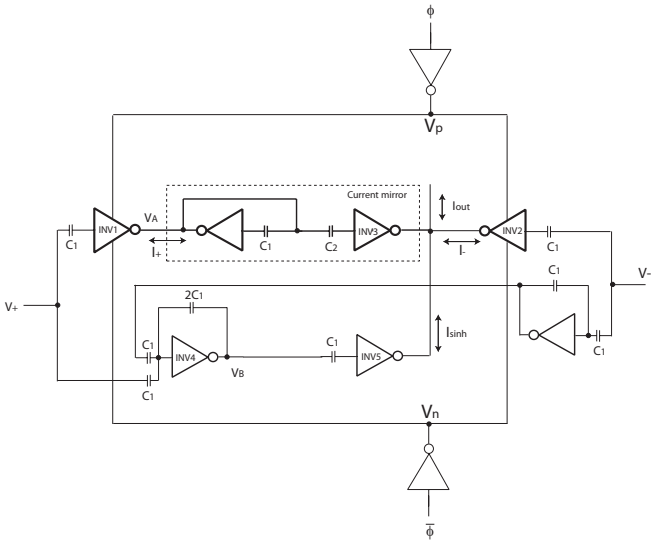

Fig. 4. *ULV transconductance amplifier.*

There are two output stages of the amplifier

1) **INV2** and **INV3**. The transconductance can be expressed as $k_1 \times \Delta V_{in}$.
2) **INV5**. The relative gain can be expressed as $k_1 \times \Delta V_B = (k_1/2) \times \Delta V_{in}$.

The output stage associated with INV5 will provide an output current which can, for ultra low supply voltages, be modelled as an $SINH$ function. This output stage resembles a standard complementary inverter. In contrast the current of the output stage associated with $INV2$ and $INV3$ resembles a $TANH$ function due to pseudo differential pair input stage. By combining the output stages we acheieve both increased transconductance and increased linearity. Simple Tayler series of the functions are given by

$$\begin{aligned} K_1 SINH(x) &= K_1 x + K_1 \frac{x^3}{3!} + ... \\ K_2 TANH(x) &= K_2 x - K_2 \frac{x^3}{3} + ... \\ K_1 SINH(x) + K_2 TANH(x) &\approx (K_1 + K_2) x \\ &\quad - \frac{(2K_2 - K_1)}{3!} x^3 \end{aligned}$$

By examining the Taylor series we observe that the increased transconductance of the combined amplifier is given by $K_1 + K_2$ which is proportional to the sum of the currents provided by the two output stages. The combined third order component is proportional to $2K_2 - K_1$.

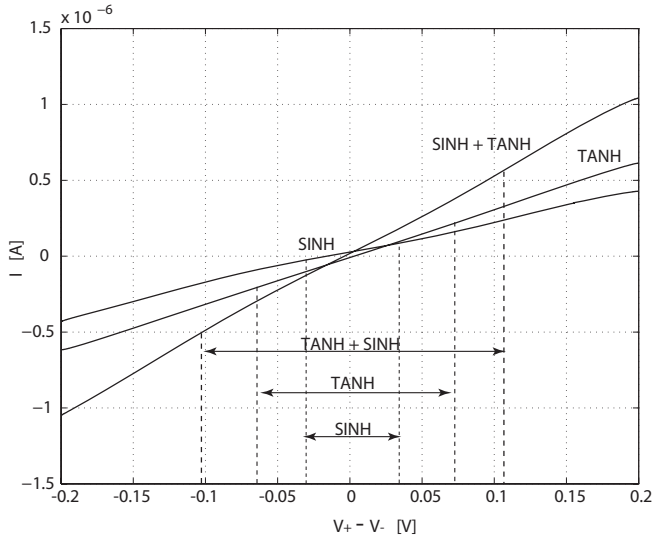

Fig. 5. *The output currents of each output stage and the combined output current. The supply voltage is* $300mV$ *and* $SINE$ *signals with an amplitude equal to* $200mV$ *are appliad to the inputs* V_+ *and* $V_–$.

The output currents of each output stage and the combined output current for a supply voltage equal to $300mV$ are shown in Fig. 5.

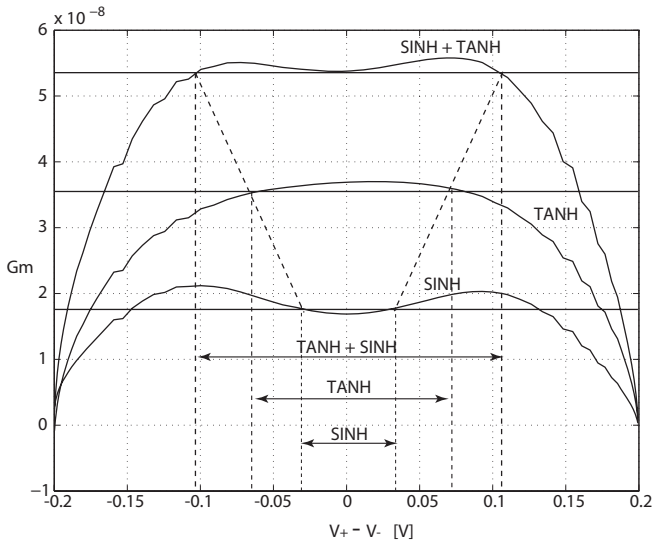

Fig. 6. *The transconductance of the two output stages and the combined output stage.*

The transconductance of the two output stages and the combined output stage are shown in Figure 6. The supply voltage used in this case is $300mV$ and the both the linear range and the transconductance are increased significantly. The pass band is dependent on the supply voltage applied. For a supply voltage equal to $250mV$ the pass band is in the range from $1.8MHz$ to $60MHz$ whereas the pass band for a supply voltage of $300mV$ is restriced to $18MHz$ and $300MHz$.

V. Conclusion

We have presented a ultra low-voltage transconductance amplifier . We may operate the amplifier with supply voltage down to $300mV$ and avoiding the traditional restrictions of low voltage analog design. The amplifier allows rail to rail signals an no need for dc-dc conversion is required. The transconductance amplifier may operate at a supply voltage equal to the threshold voltage of the nMOS transistor in a $90nm$ CMOS process.

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