World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:4, No:5, 2010

A Novel Nano-Scaled SRAM Cell

Arash Azizi Mazreah, Mohammad Reza Sahebi and Mohammad T. Manzuri Shalmani

***Abstract*—**To help overcome limits to the density of conventional SRAMs and leakage current of SRAM cell in nano-scaled CMOS technology, we have developed a four-transistor SRAM cell. The newly developed CMOS four-transistor SRAM cell uses one word-line and one bit-line during read/write operation. This cell retains its data with leakage current and positive feedback without refresh cycle. The new cell size is 19% smaller than a conventional six-transistor cell using same design rules. Also the leakage current of new cell is 60% smaller than a conventional six-transistor SRAM cell. Simulation result in 65nm CMOS technology shows new cell has correct operation during read/write operation and idle mode.

***Keywords*—**SRAM Cell, leakage current, cell area.

I. Introduction

THE on-chip caches can effectively reduce the speed gap between the processor and main memory, almost modern microprocessors employ them to boost system performance [1]. These on-chip caches are usually implemented using arrays of densely packed SRAM cells for high performance [1]. A six-transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell [2], [3]. However, the 6T cell produces a cell size an order of magnitude larger than that of a DRAM cell, which results in a low memory density [2]. In addition, as CMOS technology scaled down total leakage current of a chip increased, furthermore the total leakage current of a chip is proportional to the number of transistors of chip, and since the SRAM based on six transistor cell include large number of transistors of chip, the SRAM leakage has also become a more significant component of total chip leakage in scaled CMOS technology. Therefore, cache memory that use the six transistor SRAM cell have difficulty meeting the growing demand for a larger memory capacity in nano-scaled CMOS technology. In response to this requirement, our objective is to develop an SRAM cell with four transistors to reduce the cell area size and leakage current.

II. Novel SRAM Cell

Fig. 1 shows a circuit equivalent to a developed 4T SRAM cell using a supply voltage of 1.2V in 65-nm technology node.

Arash Azizi Mazreah is with the Islamic Azad University, Sirjan Branch, Sirjan, Iran (e-mail: aazizi@ iausirjan.ac.ir).
Mohammad Reza Sahebi is with the NICI. Company (e-mail: msaheb@nicico.com).
Mohammad T. Manzuri Shalmani is with the Computer Engineering Department, Sharif University of Technology, Tehran, Iran (e-mail: manzuri@sharif.edu).

When '0' stored in cell during idle mode, M2 and M4 are ON and there is positive feedback between ST node and STB node, therefore ST node pulled to GND by M2 and STB node pulled to V_{DD} by M4. When '1' stored in cell M3 is ON and STB pulled to GND, also M2 and M4 are OFF and for data retention without refresh operation following condition must be satisfied.

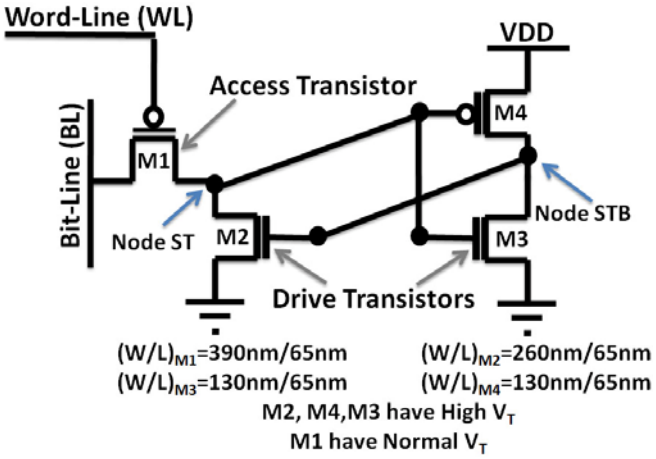

Fig. 1 Novel SRAM cell in 65-nm technology node.

Fig. 2 shows leakage current of cell during idle mode for data retention when '1' stored in cell. For satisfying above condition when '1' stored in cell during idle mode, we use leakage current of access transistor, especially sub-threshold current of access transistor ($I_{SD\text{-}M1}$ in Fig. 2) and write-bit-line maintained at V_{DD} during idle mode. For reducing leakage current that discharge ST node ($I_{DS\text{-}M2}$) when '1' stored in cell, we use high threshold voltage for driver transistor (M2) to reduce sub-threshold currents of this transistor. Since, sub-threshold current increases exponentially by decreasing threshold voltage; the leakage current of access transistors is grater than leakage current drive transistor because access transistors have lower threshold voltage. HSPICE simulation results show, with this threshold voltage assignment, above condition satisfied and '1' stored in cell successfully.

III. Write and Read Operation

When a write operation is issued the memory cell will go through the following steps.

1)-Bit-line driving: For a write, data drove on bit-line (BL), and then word-line (WL) asserted to GND.

2)-Cell flipping: this step includes two states as follows:

a)-Data is zero: in this state, ST node pulled down to low

voltage by PMOS access transistor (M1), and therefore the Load transistor (M4) will be ON, and STB node will be pulled up to V_{DD}, thus Drive transistor (M2) will be ON and positive feedback created by M2 and M4.

b)-Data is one: in this state, ST node pulled up to V_{DD} by PMOS access transistor (M1), and therefore the drive transistor (M3) will be ON , and STB node will be pulled down to GND.

3)-Idle mode: At the end of write operation, cell will go to idle mode and word-line and bit-line asserted to V_{DD}.

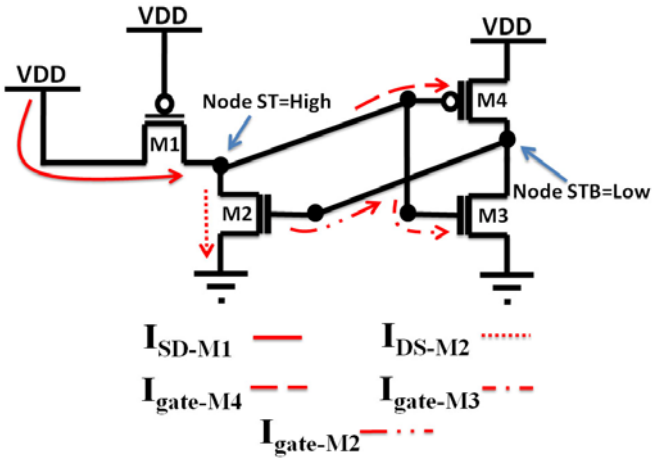

Fig. 2 Leakage current in idle mode when '1' stored in cell

When a read operation is issued the memory cell will go through the following steps.

1)-Bit-line pre-charging: For a read, bit-line charged to V_{DD}, and then floated.

2)-Word-line activation: for non-destructive read operation, in this step word-line asserted to $V_{WL\text{-}Read}$, and two states can be considered:

a)-Voltage of ST node is low: when, voltage of ST node is low, the voltage of bit-line pulled down to low voltage by M1 and M2 transistors. We refer to this voltage of bit-line as $V_{BL\text{-}Low}$.

b)-Voltage of ST node is high: when voltage of ST node is high, the voltage of bit-line and ST node equalized.

3)-Sensing: After word-line deactivate to $V_{WL\text{-}Idle}$ then sense amplifier is turned on to read data on bit-line. This new cell uses sense amplifier that introduced in [4], [5].

4)-Idle mode: At the end of read operation, cell will go to idle mode and bit-line and word-line asserted to V_{DD}.

IV. Helpful Hints

Fig. 3 shows possible layout of 4T SRAM cell in scalable CMOS design rules. Also for comparison, in Fig. 3 shows layout of 6T SRAM cell and 4T SRAM cell in scalable CMOS design rules. The 6T cell has the conventional layout topology and is as compact as possible. The 6T SRAM cell requires $416\lambda^2$ area, whereas 4T SRAM cell requires $336\lambda^2$. These numbers do not take into account the potential area reduction obtained by sharing with neighboring cells. Therefore the new cell size is 19% smaller than a conventional six-transistor cell using same design rules.

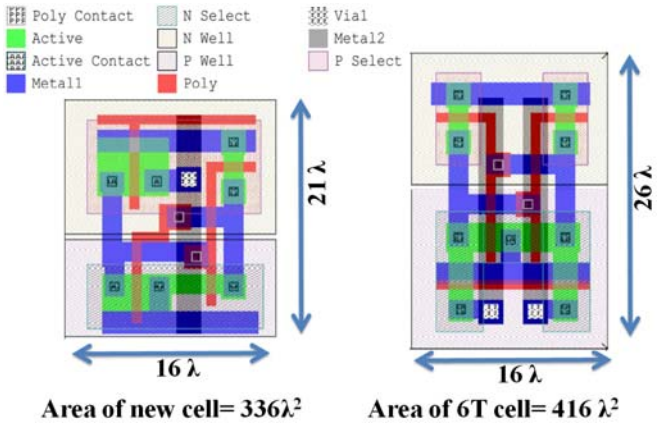

Fig. 3 Layout comparison of novel SRAM cell and Basic SRAM cell

V. Experimental Results

To verify correct operation of novel SRAM cell and comparison with conventional SRAM cell, we simulate a novel SRAM cell and conventional SRAM cell using HSPICE with 1.2V for supply voltage. Also based on layouts shown in Fig. 2, all parasitic capacitances and resistances of read/write-bit-lines, read/write-lines, bit-lines, and word-line are included in the circuit simulation. Monte Carlo analysis has been done to conventional SRAM cell and new SRAM cell to examine the impact of process variation on the leakage current and SNM (Static Noise Margin) during idle mode of these cells. Monte Carlo simulations were carried out for 1000 runs and the HSPICE parameters are obtained from the latest Predictive Technology Models (PTMs) for the technology node of 65-nm [6].

For testing the correctness of a read and write operation of novel SRAM cell, following scenario applied to new 6T SRAM cell:

a)-Writing '1' in to new cell and then read it.

b)-Writing '0' in to new cell and then read it.

Fig. 4 and Fig. 5 show simulated waveform with applying above scenario. Also based on simulation results Table I compares the novel 6T SRAM cell and Basic 6T SRAM cell. We only consider the read bit-line delays of the SRAM cells, and write delays have been ignored. The write delays of the cells are less important because we can use strong write drivers to drive the bit-lines, and write drivers are a small portion of the total SRAM [7].

TABLE I PERFORMANCE COMPARISONS OF SRAM CELLS

Metrics	Basic 6T Cell	New 4T Cell
Mean of Read Bit-line Delay (Load Capacitance=1fF)	31ps	40ps
Worst Case SNM During Idle Mode	0.25V	0.21V
Mean of Leakage Current	480nA	192nA
Area	$416\lambda^2$	$336\lambda^2$

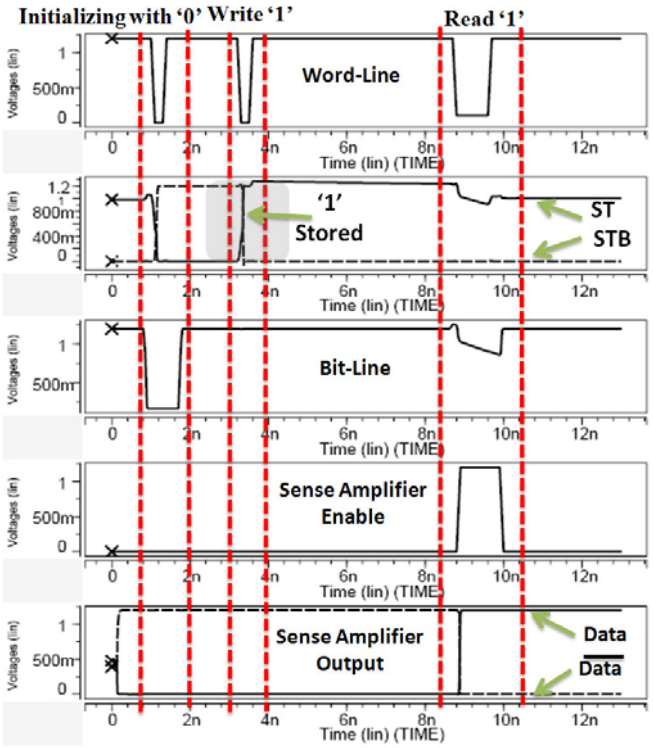

Fig. 4 Simulated waveform for writing '1' and read it

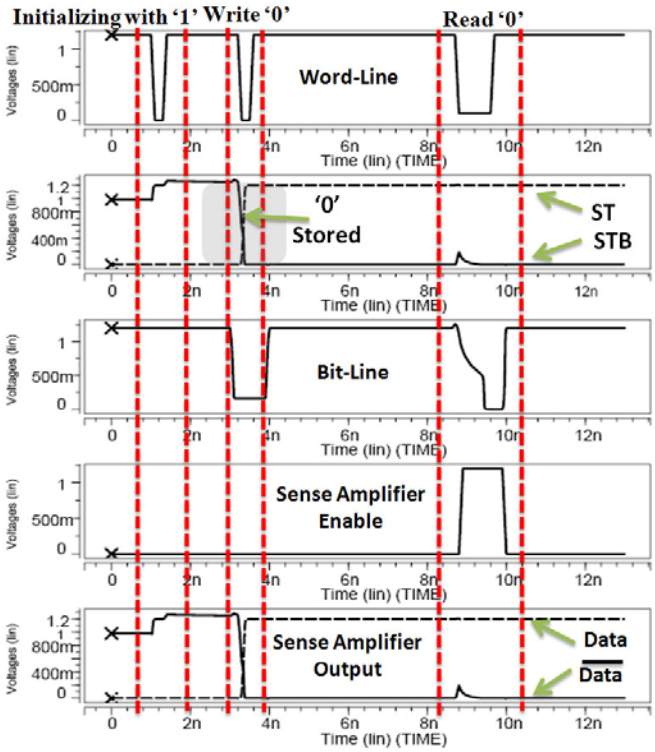

Fig. 5 Simulated waveform for writing '0' and read it

VI. Conclusion

With the aim of achieving a high density and low leakage SRAM, we developed a four transistor SRAM cell for nano-scaled CMOS technology. New cell retains its data with leakage current when there is not any positive feedback. The new cell size is 19% smaller than a 6T cell using same design rules. Leakage current of new developed SRAM cell is 60% smaller than basic 6T SRAM cell but the proposed cell is with 16% and 22% degradation in SNM and read speed, respectively.

Acknowledgment

This work is sponsored by funding from Islamic Azad University, Sirjan Branch.

References

[1] Y. J. Chang, F. Lai, and Ch. L. Yang, "Zero-Aware Asymmetric SRAM Cell for Reducing Cache Power in Writing Zero", IEEE Trans. On VLSI system, vol. 12, no. 8, pp. 827-836, August 2004.

[2] A. Kotabe et al., "A Low-Power Four-Transistor SRAM Cell With a Stacked Vertical Poly-Silicon PMOS and a Dual-Word-Voltage Scheme," IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 870-876, April 2005.

[3] B. Amelifard, F. Fallah, M. Pedram, "Low-leakage SRAM design with dual Vt transistors," 7th Int'l Symp. on Quality of Electronic Designs, 2006.

[4] A. Azizi Mazreah, M. T. Manzuri Shalmani, et al., "A novel zero-aware read-static-noise-margin-free SRAM cell for high density and high speed cache application," in Proc. 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT'08), October 2008, pp. 876–879.

[5] A. Azizi Mazreah, M. T. Manzuri et al., "A High Density and Low Power Cache Based on Novel SRAM Cell," Journal of Computers, vol. 4, no. 7, pp. 567-575, 2009.

[6] http://www.eas.asu.edu/~ptm & W. Zhao and Y. Cao, "New generation of predictive technology model for sub- 45nm design exploration," IEEE Trans. on Electron Devices, vol. 53, no. 11, pp. 2816-2823, November 2006.

[7] [8] N. Azizi, F. Najm, and A. Moshovos, "Low-leakage asymmetric-cell SRAM," IEEE Trans. on Very Large Scale Integration Systems, vol. 11, no. 4, pp. 701–715, August 2003.