

A High Time Resolution Digital Pulse Width Modulator Based on Field Programmable Gate Array's Phase Locked Loop Megafunction

Jun Wang, Tingcun Wei

Abstract—The digital pulse width modulator (DPWM) is the crucial building block for digitally-controlled DC-DC switching converter, which converts the digital duty ratio signal into its analog counterpart to control the power MOSFET transistors on or off. With the increase of switching frequency of digitally-controlled DC-DC converter, the DPWM with higher time resolution is required. In this paper, a 15-bits DPWM with three-level hybrid structure is presented; the first level is composed of a 7-bits counter and a comparator, the second one is a 5-bits delay line, and the third one is a 3-bits digital dither. The presented DPWM is designed and implemented using the PLL megafunction of FPGA (Field Programmable Gate Arrays), and the required frequency of clock signal is 128 times of switching frequency. The simulation results show that, for the switching frequency of 2 MHz, a DPWM which has the time resolution of 15 ps is achieved using a maximum clock frequency of 256MHz. The designed DPWM in this paper is especially useful for high-frequency digitally-controlled DC-DC switching converters.

Keywords—DPWM, PLL megafunction, FPGA, time resolution, digitally-controlled DC-DC switching converter.

I. INTRODUCTION

THE digitally-controlled DC-DC switching converters are widely used in the mobile phones, computers, communication equipment and so on. The DPWM is one of the important building blocks in digitally-controlled DC-DC switching converters. DPWM converts the digital duty ratio signal into its analog counterpart to control the power MOSFET transistors on or off, and in turn to regulate the output voltage. The duty ratio of the analog pulse signal is required to be proportional to the input digital value, therefore, the linearity of DPWM should be guaranteed. In addition, since usually DPWM is integrated into the controller chip, it is desired to reduce the circuit complexity and the required clock frequency.

The time resolution is an important performance of DPWM. For the digitally-controlled DC-DC switching converters, the increase of time resolution of DPWM can improve the control accuracy of output voltage [1], [2]. Moreover, with the increase of the switching frequency of DC-DC switching converter, the

switching cycle is decreased, thus the time resolution of DPWM is also needed to be increased.

Many papers have reported the methods to increase the time resolution of DPWM [3]-[12]. One method is to divide a switching cycle into time slots as fine as possible by changing the DPWM architecture. Another one is to increase the effective time resolution by using the dither, sigma-delta and slightly changing frequency. Some typical methods to increase the time resolution of DPWM are summarized as below.

A. Counter-Based Architecture

The DPWM with counter-based architecture quantize the switching cycle into 2^n time slots, and a comparator is used to select a time slot based on the input digital signal. This architecture has a good linearity, and is easy to be implemented, but it increases the power dissipation and needs a high frequency input clock [4], [5].

B. Delay Line-Based Architecture

The DPWM with delay line-based architecture also quantize the switching cycle into 2^n time slots using 2^n delay cells. This architecture increases the time resolution of DPWM by using the shorter cell delay and larger number of delay cells on the delay line. Due to mismatch of delay cells caused by process/temperature/voltage variation, the linearity of the delay line-based DPWM is worse than that of counter-based DPWM. And in addition, this kind of DPWM needs a large-scale multiplexer to choose the corresponding time slot. The advantage of this kind of DPWM is to avoid the use of high frequency input clock [5], [6].

C. Dither-Based Technology

One method of increasing the effective time resolution of DPWM is dithering technology. Dither method is based on the principle to average the output voltage within several cycles. The LSB of input digital data is changed into 1-bit (0/1) orderly and then added to the MSB of input digital data. The LC filter at power stage is used to average the output voltage, thus the effective time resolution of DPWM can be improved. However, the dither technique give rises to the output voltage ripple [7], [8].

D. Hybrid Architecture

In order to deal with the problems of above DPWM architecture, the hybrid DPWM is presented, which is the combination of two or three of above mentioned architectures [12], [13]. This architecture can balance the clock frequency

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and chip area. For example, for a DPWM with the time resolution of 10-bits, and the switching frequency is 2 MHz, if using the architecture “A”, an input clock signal with the frequency of 2 GHz is needed, which is difficult to achieve and requires large power consumption. The architecture “B” can decrease the frequency of input clock, but a large number of delay cells and large chip area are needed for realizing the fine time resolution.

The DPWM presented in this paper is with three-level hybrid architecture (A+B+C), and using the PLL megafunctions of FPGA. This feature is available in almost all FPGA, which is easy to realize the fine time resolution of DPWM.

The rest of the paper is organized as follows. Section II describes the presented DPWM architecture. Section III shows the simulation results and FPGA implementation results. Finally, Section IV gives conclusions.

II. PROPOSED DPWM ARCHITECTURE AND PRINCIPLE

In this paper a high time resolution DPWM with three-level hybrid structure is presented, the first level is composed of an n_c -bits counter and a comparator, the second one is an n_r -bits delayline, and the third one is an n_d -bits digital dither. The proposed DPWM is designed and implemented using the PLL megafunction of FPGA, and the required frequency of clock signal is 2^{n_c} times of switching frequency.

In order to demonstrate the effectiveness of above DPWM structure, a 15-bits DPWM is designed and implemented, in which the parameter of n_c , n_r and n_d are chosen to be 7, 5, 3, respectively, namely a “7-bits Counter + 5-bits PLL-delay line + 3-bits Dither” hybrid DPWM is designed. The second level is a traditional tapped delay line, five PLL blocks are used to realize 2^5 ($n_r=5$) delay-cell. The third level is a digital dither, in which the least significant 3-bits are converted into a 1-bit signal and added to the most significant 12-bits of original digital input signal, thus the effective time resolution of DPWM can be increased. And the structure of the hybrid DPWM is shown in Fig. 1.

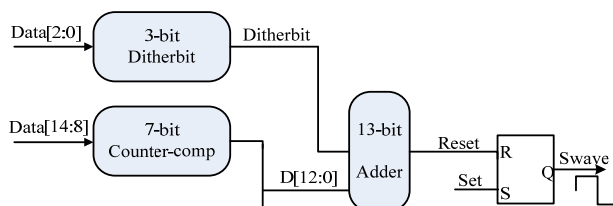


Fig. 1 Structure of 15-bits hybrid DPWM presented in this paper

The hybrid DPWM utilizes the PLL megafunction of FPGA, which can realize the function of phase shifting (50% duty cycle), frequency division, and frequency multiplication. As shown in Fig. 2, the first PLL megafunction converts the input clock into the needed frequency of 256 MHz, And Ck0, Ck90, Ck180, Ck270 realizes the phase shifting of 0° , 90° , 180° , 270° of 256MHz signal. Then the same four PLL megafunctions use

the new shifting clock as input clock to achieve eight constant phase shifting of $11^\circ 25'$ ($90^\circ/8$). Through this way a cycle of 256 MHz signal can be equally divided into 32 time slots and every portion is 122ps.

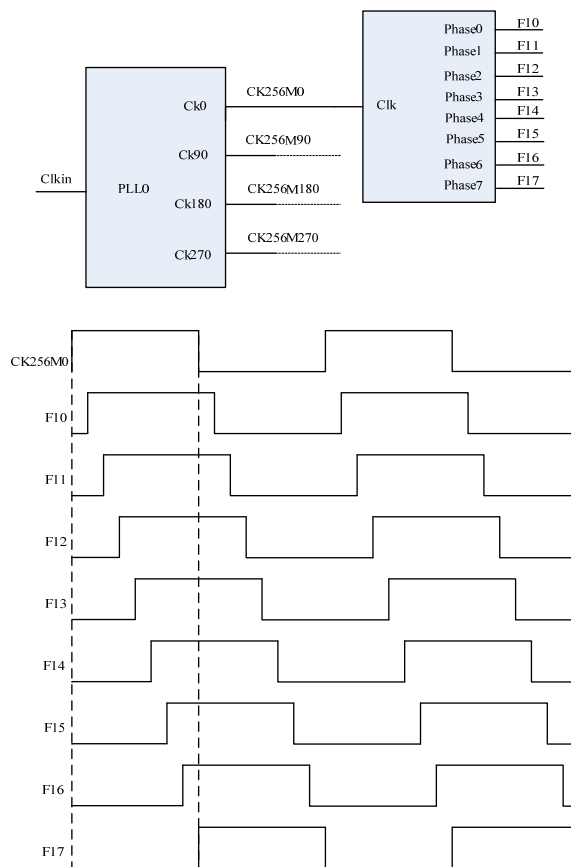


Fig. 2 5-bit PLL megafunction structure and phase shifting

The third level uses the digital dither. The idea of digital dither is changing the duty cycle by the LSB bits over a few switching cycles. The LSB Data [2:0] are converted into 1-bit and added to the most significant 12-bits of original input signal, the final duty ratio has a value between two close quantized duty ratios, so the effective time resolution of DPWM can be increased. And the dither sequence is shown in Table I, a look up table stores 2^3 dither sequences, each sequence is with 2^3 -bit long [7].

3bits LSB	Dither Sequence
000	00000000
001	00000001
010	00010001
011	00100101
100	01010101
101	01011011
110	01110111
111	01111111

The presented DPWM structure has several advantages: 1) the use of PLL megafunction is convenient, and can easily

realize the fine phase shifting of the clock to decrease the time step, and increase the time resolution of DPWM; 2) three-level hybrid architecture balance the counter frequency and the circuit scale.

III. SIMULATION RESULTS AND FPGA IMPLEMENTATION

In order to verify this architecture, the DPWM is implemented on Cyclone V FPGA. And all the modules of the hybrid-based DPWM are design in Verilog-HDL, the simulation tools are Quartus II and Modelsim. The external clock frequency is 50 MHz, and the switching frequency is 2 MHz. Fig. 3 shows the simulation results when input data are 5'd22211, the LSB 3'b011 is changed to 1-bit in eight clock

cycles orderly and then added to the MSB 4'd2776 of input data. The duty ratio of ideal input data is 67.78%, and equals to the average of eight clock cycles based on the dither principle.

$$\frac{22211}{2^{15}} = 67.78\% \quad (1)$$

$$\frac{2776 * 5 + 2777 * 3}{2^{12}} = 67.78\% \quad (2)$$

Equations (1) and (2) show corresponding relationship between 15-bit input data and 12-bit transformed data, they are equivalent.

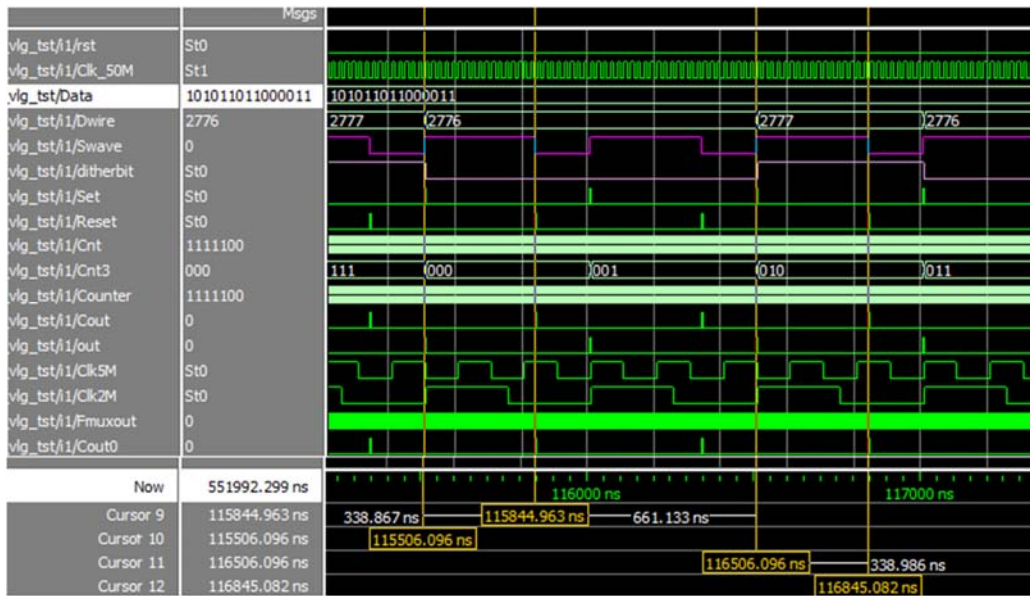


Fig. 3 Simulation results using Modelsim

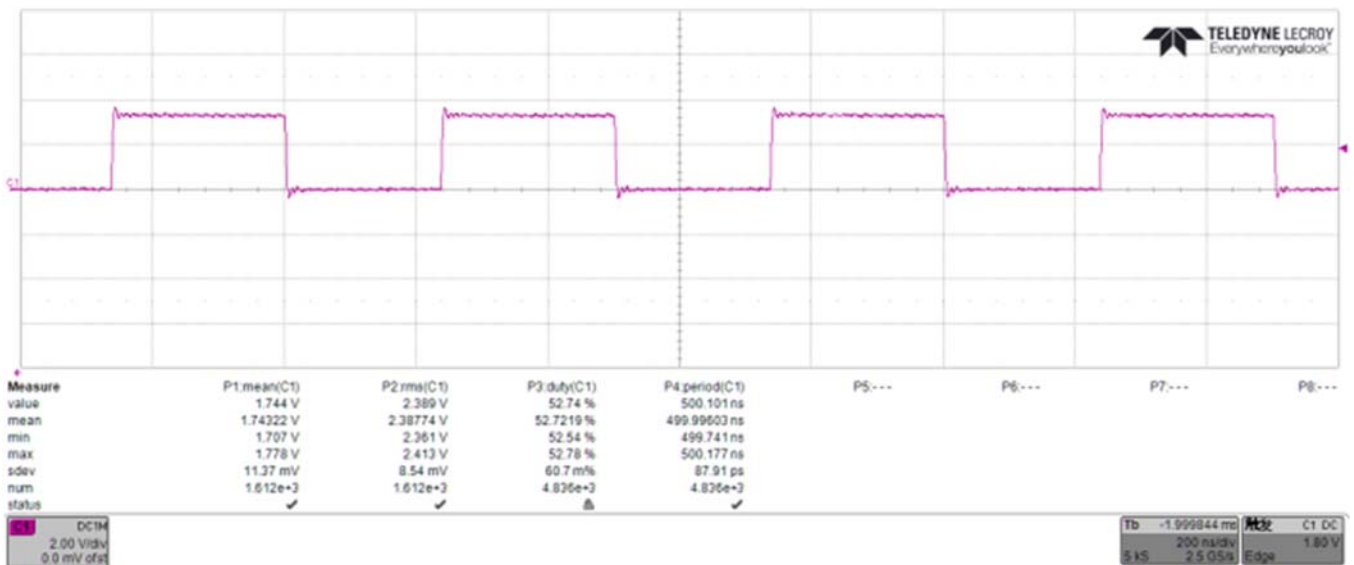


Fig. 4 Output duty ratio when input data=4295

From the simulation results, the duty ratio is calculated as:

$$\frac{333.876 \times 5 + 338.986 \times 3}{8} \text{ ns} / 500 \text{ ns} = 67.78\% \quad (3)$$

which is same with the ideal duty ratio. This simulation confirms the feasibility of this structure and a time resolution of 15 ps can be obtained because of the fine phase shifting produced by PLL megafunction.

Based on this architecture, a 13-bits DPWM is designed and implemented on Cyclone V FPGA, in which the three-level architecture are “5-bits Counter + 5-bits PLL-delay line + 3-bits Dither”. Because of the max frequency limit of PLL megafunction in Cyclone V FPGA, the 13-bits DPWM is adopted. When input data is 4’d4295, the experiment result is shown in Fig. 4. From this picture, it can be seen that, the duty ratio is 52.74%, and which is only with 0.17% error comparing with ideal duty ratio of 52.43% shown in (4):

$$\frac{4295}{2^{13}} = 52.43\% \quad (4)$$

The duty ratio of output wave can be observed in oscilloscope, the relationship between the duty ratio and input data can be easily observed from Fig. 5. Fig. 5 shows the measurement results of duty ratio when input data [12:0] changing from 4’d0000 to 4’d8192. As can be seen from Fig. 5, the DPWM have a nearly perfect linearity. The measurement results show that the duty ratio is increasing well with the increase of input data. Theoretically, the PLL megafunction can realize fine phase shifting, and achieve accurate delay time.

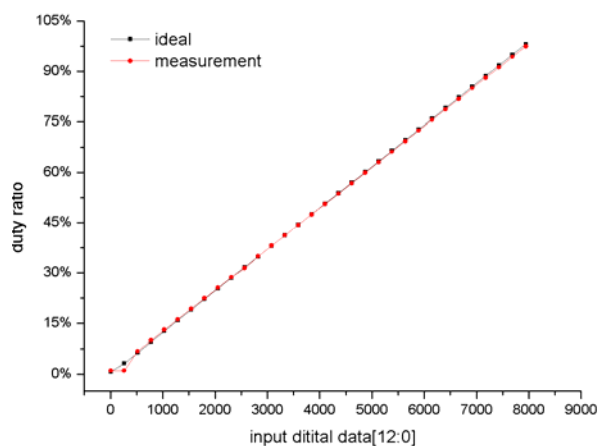


Fig. 5 Relationship between input data and the duty ratio

IV. CONCLUSION

In this paper, we present a three-level hybrid DPWM with “7-bits Counter+ 5-bits PLL-delayline + 3-bits Dither” architecture. The switching frequency of 2 MHz and the time resolution of 15 ps can be obtained with a maximum clock frequency of 256 MHz. The PLL megafunction is used to realize fine phase shifting. And a 13-bits DPWM which has the

same structure is designed and implemented on Cyclone V FPGA. The measurements results show that the presented DPWM can achieve good linearity.

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