

On-Chip Aging Sensor Circuit Based on Phase Locked Loop Circuit

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Abstract : In sub micrometer technology, the aging phenomenon starts to have a significant impact on the reliability of integrated circuits by bringing performance degradation. For that reason, it is important to have a capability to evaluate the aging effects accurately. This paper presents an accurate aging measurement approach based on phase-locked loop (PLL) and voltage-controlled oscillator (VCO) circuit. The architecture is rejecting the circuit self-aging effect from the characteristics of PLL, which is generating the frequency without any aging phenomena affects. The aging monitor is implemented in low power 32 nm CMOS technology, and occupies a pretty small area. Aging simulation results show that the proposed aging measurement circuit improves accuracy by about 2.8% at high temperature and 19.6% at high voltage.

Keywords : aging effect, HCI, NBTI, nanoscale

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