

Analysis of Stacked SCR-Based ESD Protection Circuit with Low Trigger Voltage and Latch-Up Immunity

Authors : Jun-Geol Park, Kyoung-Il Do, Min-Ju Kwon, Kyung-Hyun Park, Yong-Seo Koo

Abstract : In this paper, we proposed the SCR (Silicon Controlled Rectifier)-based ESD (Electrostatic Discharge) protection circuit for latch-up immunity. The proposed circuit has a lower trigger voltage and a higher holding voltage characteristic by using the zener diode structure. These characteristics prevent latch-up problem in normal operating conditions. The proposed circuit was analyzed to figure out the electrical characteristics by the variations of design parameters D1, D2 and stack technology to obtain the n-fold electrical characteristics. The simulations are accomplished by using the Synopsys TCAD simulator. When using the stack technology, 2-stack has the holding voltage of 6.9V and 3-stack has the holding voltage of 10.9V.

Keywords : ESD, SCR, trigger voltage, holding voltage

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