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A Power-Gating Scheme to Reduce Leakage Power for P-type Adiabatic Logic Circuits

Hong Li, Linfeng Li, and Jianping Hu

***Abstract*—**With rapid technology scaling, the proportion of the static power consumption catches up with dynamic power consumption gradually. To decrease leakage consumption is becoming more and more important in low-power design. This paper presents a power-gating scheme for P-DTGAL (p-type dual transmission gate adiabatic logic) circuits to reduce leakage power dissipations under deep submicron process. The energy dissipations of P-DTGAL circuits with power-gating scheme are investigated in different processes, frequencies and active ratios. BSIM4 model is adopted to reflect the characteristics of the leakage currents. HSPICE simulations show that the leakage loss is greatly reduced by using the P-DTGAL with power-gating techniques.

***Keywords*—**Leakage reduction, low power, deep submicron CMOS circuits, P-type adiabatic circuits.

I. Introduction

BEFORE the CMOS process is scaled into deep sub-micro process, dynamic energy loss has always dominated power consumption, while leakage dissipation is little. The aggressive scaling of device dimensions and threshold voltage has significantly increased leakage current exponentially, thus the MOS devices will no longer be totally turned-off anymore. The power dissipation caused by leakage current can't be neglected anymore, which attracts extensive attentions [1]–[5].

There are several sources of leakage currents: sub-threshold leakage current due to very low threshold voltage (V_T), gate leakage current due to very thin gate oxide (T_{OX}), and band-to-band tunneling leakage current due to heavily-doped halo [1]–[3]. Several leakage reduction techniques, such as dual threshold CMOS, power gating technique, stacking transistor techniques, variable threshold CMOS, and input vector control have been proposed in recent years and achieved considerable energy savings [1]–[5].

Adiabatic logic is an attractive low-power approach by utilizing AC voltage supplies (power-clocks) to recycle the energy of circuits instead of being dissipated as heat. Several adiabatic logic families and their applications have been reported and achieved considerable energy savings [6], [7]. Similar to power-gating techniques of conventional CMOS circuits, power-gating schemes for adiabatic circuits have been also introduced to reduce dynamic energy dissipations during idle periods [8], [9].

Base on the pact that PMOS transistors have an order of magnitude smaller gate leakage than NMOS ones, P-type CMOS design technology has been proposed to reduce the leakage power [10]. However, the previously reported P-type CMOS design technology is only investigated for conventional CMOS circuits. To the best of our knowledge, no previous investigates for leakage reductions of P-type adiabatic circuits with the power-gating approaches are presented.

This paper focuses on leakage reduction of adiabatic circuits using P-type power-gating schemes in scaled CMOS processes. A P-type power-gating scheme for P-DTGAL (P-type dual transmission gate adiabatic logic) circuits is proposed. Further, the leakage reductions of P-DTGAL circuits with the proposed P-type power-gating scheme are investigated. Taken as an example, power dissipations of an 8-bit full adder based on P-DTGAL circuits with the proposed P-type power-gating scheme are investigated in different processes, frequencies and active ratios. BSIM4 model [11] is adopted to reflect the characteristics of the leakage currents. HSPICE simulations show that the 8-bit adiabatic full adder with the P-type power-gating scheme shows significant improvement in terms of leakage power consumptions in deep sub-micron process.

II. Review of Dual Transmission Gate Adiabatic Logic

The typical adiabatic circuit 2N-2N2P is showed in Fig. 1(a) [12]. 2P-2P2N is a complementary logic, and its structure and operation are complementary to the 2N-2N2P, as shown in Fig. 1(b) [7]. Cascaded 2N-2N2P and 2P-2P2N gates are driven by the four-phase power clocks, as shown in Fig. 1(c). Their simulated waveforms are shown Fig. 1(d). It can be seen that they have non-adiabatic energy loss on output nodes, which is dependent on the load capacitance. Therefore, if they are used for driving large load capacitance, non-adiabatic energy loss is large. For quasi-adiabatic circuits such as ECRL (Efficient Charge Recovery Logic) and PAL-2N (Pass-transistor adiabatic logic with NMOS pull-down configuration) etc, the same conclusion can be obtained [6], [13].

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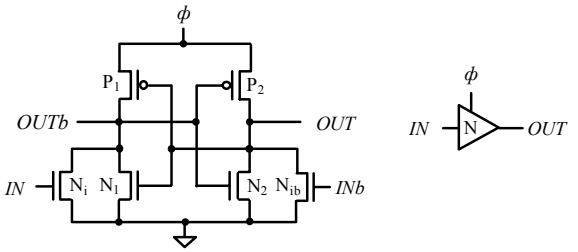
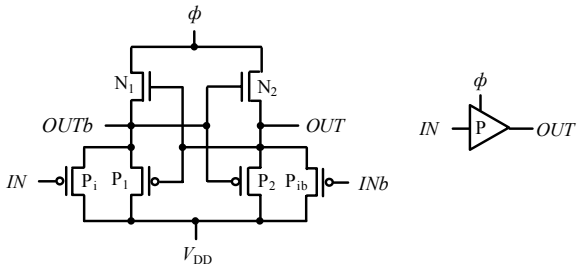
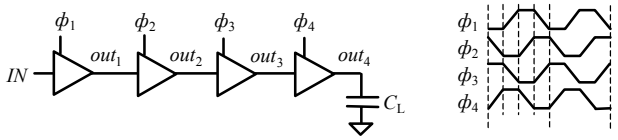


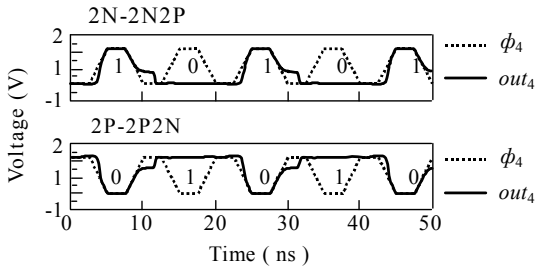
(a) 2N-2N2P and symbol



(b) 2P-2P2N and symbol



(c) Buffer chain and power clock



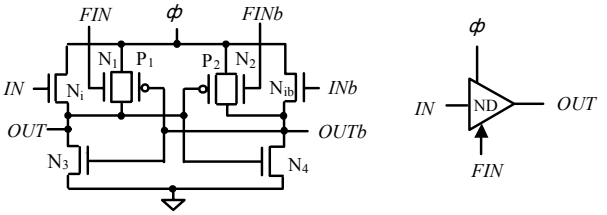
(d) Simulated waveforms

Fig. 1 2N-2N2P and 2P-2P-2N buffers

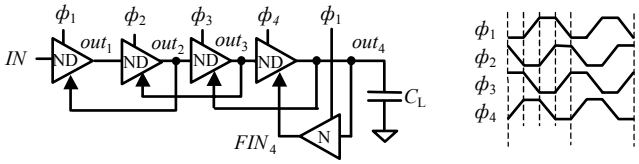
To overcome this disadvantage, a N-type dual transmission gate adiabatic logic (N-DTGAL) was presented in [14], as shown in Fig. 2. The power-clock ϕ charges the output (*OUT* or *OUTb*) through N_i and P_1 (or N_{ib} and P_2) by control of the inputs (*IN* and *INB*). The energy of output nodes is recovered to ϕ through N_1 and P_1 (or N_2 and P_2) by control of the feedback signals (*FIN* and *FINb*), which are from the outputs of the next-stage buffer. For the final-stage N-DTGAL gate in a pipelined chain, an additional 2N-2N2P buffer is used and its outputs (FIN_4 and $FINb_4$) control energy-recovery of the final-stage N-DTGAL gate.

A P-type DTGAL has also been reported in [7], as shown in Fig. 3. Its structure, operation, and signal waveforms are complementary to the N-type DTGAL. For the final-stage P-DTGAL gate in a pipelined chain, an additional 2P-2P2N buffer is used and its outputs (FIN_4 and $FINb_4$) control energy-recovery of the final-stage P-DTGAL gate. Cascaded P-DTGAL and N-DTGAL gates are driven by the same four-phase power-clocks as the 2N-2N2P.

The simulated waveforms for the P-DTGAL and N-DTGAL circuits are shown Fig. 4. It can be seen that N-DTGAL and P-DTGAL haven't non-adiabatic loss on output loads. Although the additional 2N-2N2P (or 2P-2P-2N) buffer has the non-adiabatic energy loss CV_{TP}^2 (or CV_{TN}^2), this energy loss is small, because the capacitance C, which mainly consists of gate capacitance of input transistors in the N-DTGAL and P-DTGAL buffers, is far smaller than the load capacitance (C_L) of the logic circuits [7], [14].

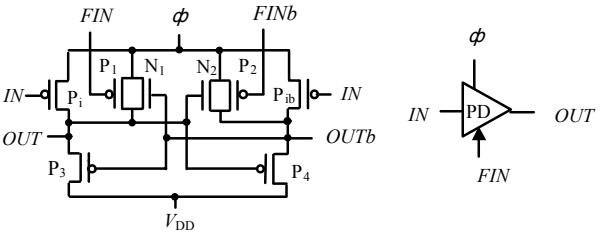


(a) Schematic and symbol

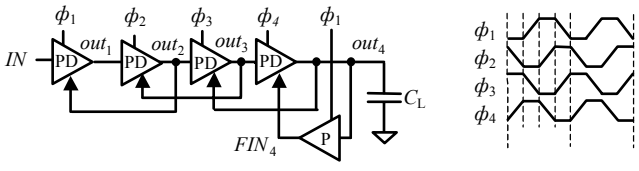


(b) Buffer chain and power clock

Fig. 2 N-type DTGAL buffer



(a) Schematic and symbol



(b) Buffer chain and power clock

Fig. 3 P-type DTGAL buffer

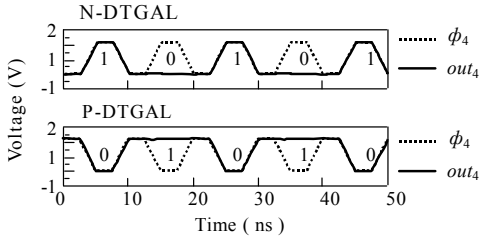


Fig. 4 Simulated waveforms for N-DTGAL and P-DTGAL buffers

III. Power-Gating Scheme for P-type Dual Transmission Gate Adiabatic Logic Circuits

The proposed power-gating scheme for P-DTGAL circuits is shown in Fig. 5. The power-gating switches using a P-DTGAL buffer chain with large device sizes are inserted between power-clocks ($\phi_1 - \phi_4$) and virtual power-clocks ($pc_1 - pc_4$). They are used to disconnect the P-type adiabatic logic block from the power-clocks during idle periods.

The simulated waveforms for the power-gating adiabatic circuits are shown in Fig. 6. The power-gated adiabatic circuits work in two modes under the control of *Sleep* (sleep enable signal). In sleep mode, *Sleep* is high, thus virtual power-clocks ($pc_1 - pc_4$) are set as high level, so that the power-gated adiabatic logic block is shut down to reduce its energy dissipation. In active mode, *Sleep* is low, thus virtual power-clocks ($pc_1 - pc_4$) follow power-clocks ($\phi_1 - \phi_4$), and the power-gated adiabatic logic block works as usual.

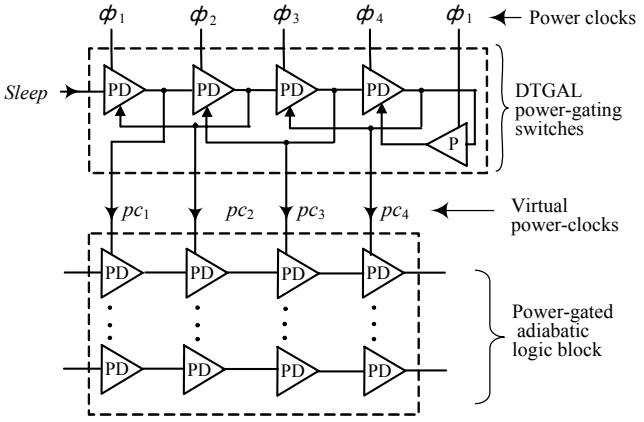


Fig. 5 Power-gating scheme for PDTGAL circuits

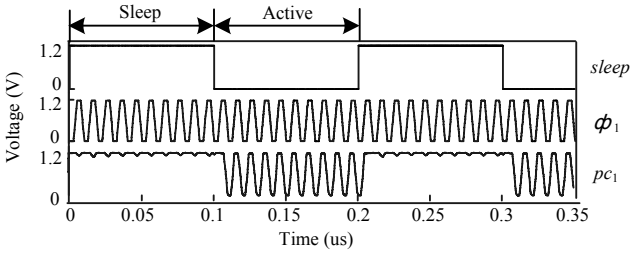
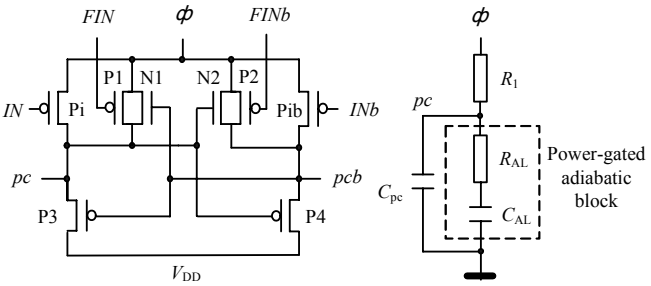


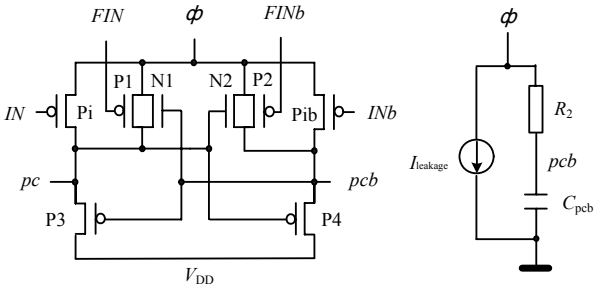
Fig. 6 Simulation waveforms of power-gating adiabatic circuits

IV. Energy Dissipations of Power-Gating Switches

The power-gating switches introduce an additional energy loss, which can be analyzed by using the equivalent circuit of the power-gating switch shown in Fig. 7.



(a) Equivalent circuit of power-gating switch in active mode



(b) Equivalent circuit of power-gating switch in sleep mode

Fig. 7 Equivalent circuits of the power-gating switch

In active mode, the power-gated logic block can be modeled by a capacitor C_{AL} and a resistor R_{AL} [15]. The transmission-gate TG1 (Pi, N1, and P1) is on, and R_1 is its turn-on resistance, which is in inverse proportion to the channel width of TG1. C_{pc} is capacitance of the node *pc*, and it includes wire capacitance and the input capacitance of the next-stage P-type power-gating switch, which is proportional to the channel width of TG1. The transmission-gate TG2 (Pib, N2, and P2) is off. The energy loss per cycle in active mode introduced by the power-gating switch can be written as

$$E_{\text{active}} = \left(\frac{2R_1C_{\text{AL}}}{T/4}\right)C_{\text{AL}}V_{\text{DD}}{}^2 + \left(\frac{2R_1C_{\text{pc}}}{T/4}\right)C_{\text{PC}}V_{\text{DD}}{}^2, \quad (1)$$

where T and V_{DD} are period and peak-to-peak voltage of power clocks. The first term is energy loss for supplying the power-gating adiabatic logic block, and the second term is energy loss for driving the next-stage and previous-stage P-DTGAL power-gating switches.

In sleep mode, TG1 is off, and $I_{leakage}$ is its leakage current. TG2 is on, and R_2 is its turn-on resistance, which is in inverse proportion to the channel width of TG2. The energy loss per cycle in sleep mode introduced by the power-gating switch can be written as:

$$E_{\text{sleep}} = I_{\text{leakage}} T + (\frac{2R_2 C_{\text{pcb}}}{T/4}) C_{\text{pcb}} {V_{\text{DD}}}^2 \quad (2)$$

The first term proportional to the channel width of TG1 is leakage energy loss of TG1. The second term is energy loss for charging and discharging node *pcb*.

Total average energy loss per cycle is written as:

$$E_{\text{AV}} = \frac{(E_{\text{active}})(T_{\text{active}}) + E_{\text{sleep}}(T_{\text{sleep}})}{(T_{\text{active}} + T_{\text{sleep}})} = (E_{\text{active}})\alpha + E_{\text{sleep}}(1-\alpha) \quad (3)$$

where T_{active} is active time, T_{sleep} is sleep time, and $\alpha = T_{active}/(T_{active} + T_{sleep})$ is active ratio.

V. Optimization for Energy Dissipations of Power-Gating Switches in Different CMOS Processes

According to (1), E_{active} can be reduced by increasing channel width of TG1, because turn-on resistance R_1 of TG1 is reduced. However, for a large channel width of TG1, E_{active} will be increased since C_{PC} is proportional to the channel width of TG1. Therefore, E_{active} can be minimized by choosing optimal sizes of TG1. Fig. 8 and Fig. 9 show the energy dissipation (E_{active}) of the power-gating switch for various channel widths of TG1 in 0.09um and 0.045um process, respectively.

According to (2), E_{sleep} can be reduced by reducing R_2 and C_{pcb}, which are in inverse proportion to and proportional to the channel width of TG2, respectively. Fig. 10 and Fig. 11 show the energy dissipation (E_{sleep}) per cycle of the power-gating switch for various channel widths of TG1 in 0.09um and 0.045um processes, respectively. In this simulations, the device size of the transistors (Pib, and P2) have been taken as an optimal size with W/L = 12λ/2λ, and the transistor N2 is also taken as W/L = 12λ/2λ. For 0.09um and 0.045um processes, λ=0.09μm and 0.026μm, respectively.

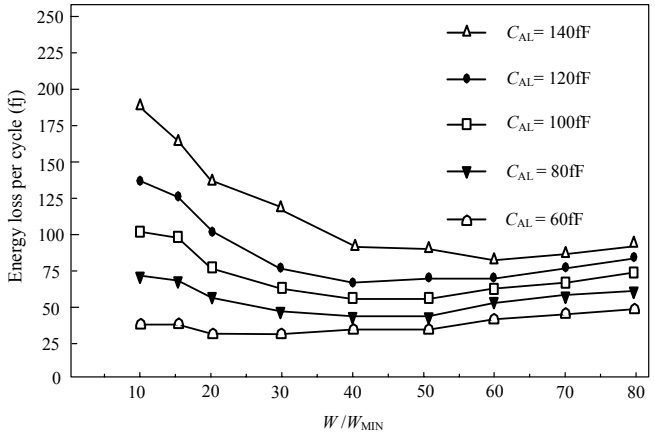


Fig. 8 Energy dissipation (E_{active}) of the power-gating switch in active mode versus channel width of the transistors (Ni and N1) in 90nm process. W is channel width of transistors (Ni and N1), and W_{MIN} = 0.135μm. The channel width of the transistor P1 are two times as large as Ni and N1. f is 200MHz and V_{DD} is 1.2V

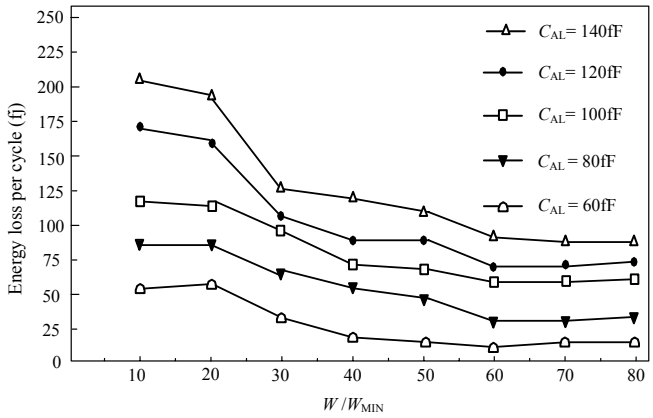


Fig. 9 Energy dissipation (E_{active}) of the power-gating switch in active mode versus channel width of the transistors (Ni and N1)in 45nm process. W is channel width of transistors (Ni and N1), and W_{MIN} = 0.069μm. The channel width of the transistor P1 are two times as large as Ni and N1. f is 400MHz and V_{DD} is 1.0V

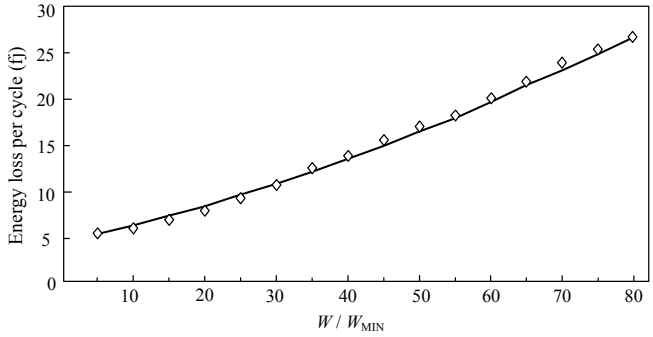


Fig. 10 Energy dissipation (E_{sleep}) of the power-gating switch in sleep mode versus channel width of the transistors (Ni and N1) in 90nm process. W is channel width of transistors (Ni and N1), and W_{MIN} = 0.135μm. The channel width of the transistor P1 are two times as large as Ni and N1. f is 200MHz and V_{DD} is 1.2V

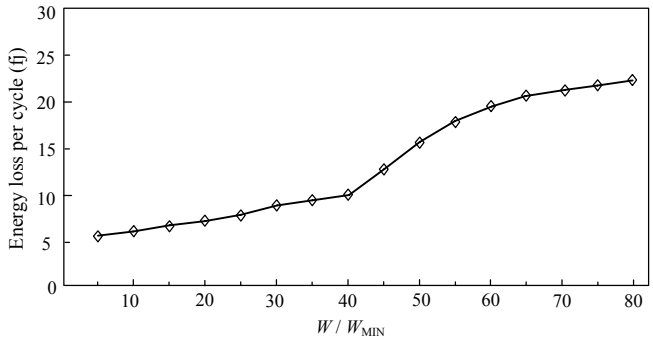


Fig. 11 Energy dissipation (E_{sleep}) of the power-gating switch in sleep mode versus channel width of the transistors (Ni and N1) in 45nm process. W is channel width of transistors (Ni and N1), and W_{MIN} = 0.069μm. The channel width of the transistor P1 are two times as large as Ni and N1. f is 400MHz and V_{DD} is 1.0V

The total energy overhead of the power-gating switches can be minimized by choosing optimal sizes of TG1 according (1) to (3) for a given process, active ratio, and the power-gated adiabatic block.

VI. Leakage Reduction of 8-bit Full Adder Based on P-DTGAL Circuits Using Power-Gating Scheme

We use an 8-bit carry-lookahead adder (CLA) to show the leakage reduction of P-DTGAL power-gating circuits in deep submicron process, which is shown in Fig. 12. The power-gating switches with six-stage P-DTGAL buffer chain are inserted between power-clocks (ϕ_1 –ϕ_4) and virtual power-clocks (pc_1 – pc_6) to maintain proper pipelining operation. The phase of virtual power-clocks (pc_5 and pc_6) is the same as ϕ_1 and ϕ_2, respectively.

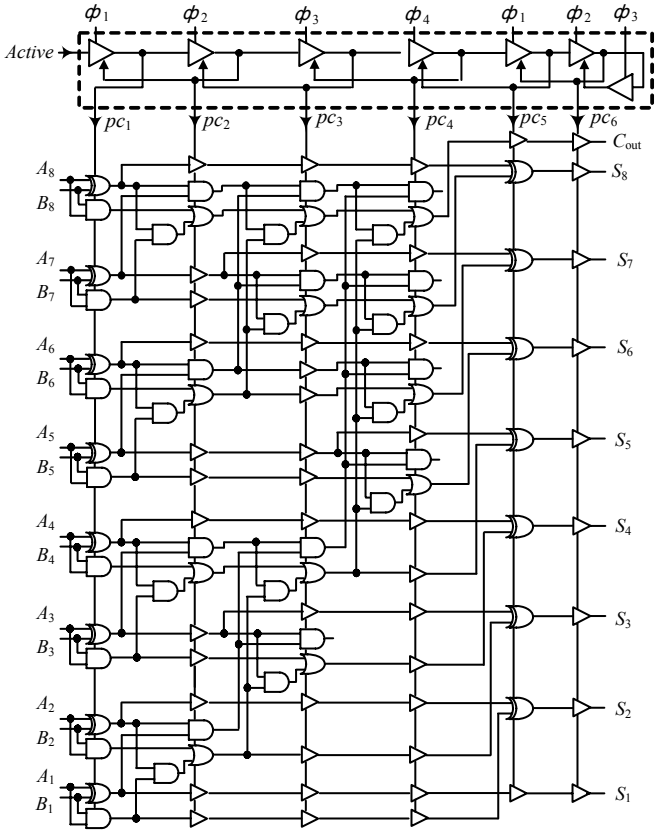


Fig. 12 8-bit full adder based on P-DTGAL circuits using power-gating technique

The logic gates used in the adder are realized with P-DTGAL circuits by using the PMOS pass-transistor logic block to replace the transistors (P_i and P_{ib}) of Fig. 3(a), as shown in Fig. 13. In Fig. 13, only the P-logic input blocks are shown and the other transistors are omitted for simplicity.

In order to extract the equivalent capacitor C_{AL} of the 8-bit adder based on P-DTGAL circuits for each power-clock, the simulation tests have been performed. The optimizations for the power-gating switches have also been carried out according to (3) with a given active ratio (a = 0.2).

Considering the energy overhead of the power-gating switches and acceptable area penalty. For the 90nm process, the channel width of the transistors (Pi and P1) of all P-DTGAL power-gating switches are taken with $40W_{MIN}$ (5.4μm), and the channel width of the transistors (N2, Pib and P2) is taken an optimal size with W/L = 12λ/2λ and λ=0.045μm. For the 45nm process, the channel width of the transistors (Pi and P1) of all P-DTGAL power-gating switches are taken with $60W_{MIN}$ (4.14μm), and the channel width of the transistors (N2, Pib and P2) is taken an optimal size with W/L = 12λ/2λ and λ=0.023μm.

The function verifications and energy loss tests have been carried out for the 8-bit full adder with power-gating switches in different processes, frequencies and active ratios. At 90nm process, the total power consumption and leakage power consumption of the 8bit full adder with power-gating switches are shown in Table I and Table II, respectively. At 45nm process, the total power consumption and leakage power consumption of the 8bit full adder with power-gating switches are shown in Table III and Table IV.

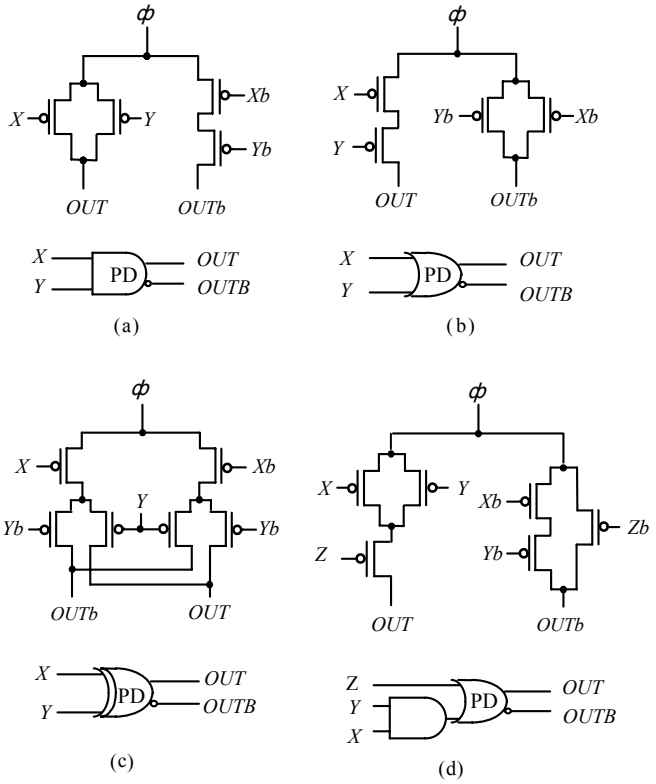


Fig. 13 Logic gates based on P-DTGAL circuits used in the 8-bit full adder

For comparison, an 8-bit full adder based on static CMOS logic circuits is also simulated. Fig. 14 shows saving rate of leakage consumption of the 8-bit full adder with the P-DTGAL power-gating switches to static CMOS implementation, which are 73.1% to 79.5% and 82% to 89.6% for clock rates ranging from 100 to 300MHz at a = 0.005 in 90nm process and 45nm process, respectively. The 8-bit adiabatic full adder using P-DTGAL power-gating schemes obtain more leakage loss savings in 45m CMOS process than 90nm CMOS process.

TABLE I
TOTAL POWER CONSUMPTION OF THE ADIABATIC 8-BIT CLA AT 90NM CMOS PROCESS (μW)

Operation Frequency (MHz)	ACTIVE RATIO			
	0.005	0.01	0.02	0.03
100	2.349	2.698	3.396	4.014
200	6.611	7.422	8.799	10.434
300	7.57	9.14	12.28	15.18

TABLE II
LEAKAGE POWER CONSUMPTION OF THE ADIABATIC 8-BIT CLA AT 90NM CMOS PROCESS (μW)

Operation Frequency (MHz)	ACTIVE RATIO			
	0.005	0.01	0.02	0.03
100	1.99	1.98	1.96	1.86
200	5.771	5.742	5.439	5.394
300	5.97	5.94	5.88	5.58

TABLE III
TOTAL POWER CONSUMPTION OF THE ADIABATIC 8-BIT CLA AT 45NM CMOS PROCESS (μW)

Operation Frequency (MHz)	ACTIVE RATIO			
	0.005	0.01	0.02	0.03
100	1.494	1.788	2.376	2.916
200	2.74	3.48	3.76	6.36
300	3.041	5.282	7.764	10.134

TABLE IV
LEAKAGE POWER CONSUMPTION OF THE ADIABATIC 8-BIT CLA AT 45NM CMOS PROCESS (μW)

Operation Frequency (MHz)	ACTIVE RATIO			
	0.005	0.01	0.02	0.03
100	1.194	1.188	1.176	1.116
200	1.99	1.98	1.96	1.86
300	2.786	2.772	2.744	2.604

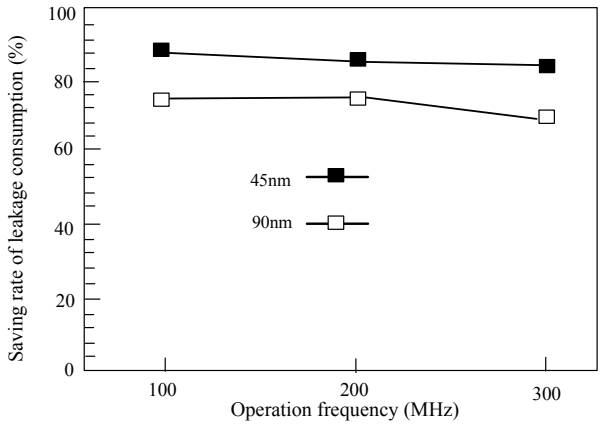


Fig. 14 Saving rate of leakage loss of the P-DTGAL 8-bit full adder with power-gating to static CMOS implementation in 90nm process and 45nm processes. Active ratio (a) = 0.005.

As can be seen from Fig. 14, with the scaling of device dimensions, more leakage loss can be saved by using the P-type adiabatic power-gating techniques, because both sub-threshold leakage and gate leakage of the P-type adiabatic circuits are all reduced compared with static ones.

VII. CONCLUSION

In this paper, the adiabatic circuits with P-DTGAL power-gating techniques are investigated in terms of leakage power loss. The results show that the leakage loss of the adiabatic circuits can be reduced effectively by using P-DTGAL power-gating techniques.

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