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Dynamic Variation in Nano-Scale CMOS SRAM Cells Due to LF/RTS Noise and Threshold Voltage

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Abstract : The dynamic variation in memory devices such as the Static Random Access Memory can give errors in read or write operations. In this paper, the effect of low-frequency and random telegraph noise on the dynamic variation of one SRAM cell is detailed. The effect on circuit noise, speed, and length of time of processing is examined, using the Supply Read Retention Voltage and the Read Static Noise Margin. New test run methods are also developed. The obtained results simulation shows the importance of noise caused by dynamic variation, and the impact of Random Telegraph noise on SRAM variability is examined by evaluating the statistical distributions of Random Telegraph noise amplitude in the pull-up, pull-down. The threshold voltage mismatch between neighboring cell transistors due to intrinsic fluctuations typically contributes to larger reductions in static noise margin. Also the contribution of each of the SRAM transistor to total dynamic variation has been identified.

Keywords : low-frequency noise, random telegraph noise, dynamic variation, SRRV
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