World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:13, No:06, 2019

Digital Encoder Based Power Frequency Deviation Measurement

Authors : Syed Javed Arif, Mohd Ayyub Khan, Saleem Anwar Khan

Abstract : In this paper, a simple method is presented for measurement of power frequency deviations. A phase locked loop (PLL) is used to multiply the signal under test by a factor of 100. The number of pulses in this pulse train signal is counted over a stable known period, using decade driving assemblies (DDAs) and flip-flops. These signals are combined using logic gates and then passed through decade counters to give a unique combination of pulses or levels, which are further encoded. These pulses are equally suitable for both control applications and display units. The experimental circuit developed gives a resolution of 1 Hz within the measurement period of 20 ms. The proposed circuit is also simulated in Verilog Hardware Description Language (VHDL) and implemented using Field Programing Gate Arrays (FPGAs). A Mixed signal Oscilloscope (MSO) is used to observe the results of FPGA implementation. These results are compared with the results of the proposed circuit of discrete components. The proposed system is useful for frequency deviation measurement and control in power systems.

Keywords : frequency measurement, digital control, phase locked loop, encoder, Verilog HDL
Conference Title : ICECEEM 2019 : International Conference on Electronics, Communication Engineering and Electronic Media
Conference Location : Toronto, Canada
Conference Dates : June 17-18, 2019