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Timing and Noise Data Mining Algorithm and Software Tool in Very Large Scale Integration (VLSI) Design

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Abstract : Very Large Scale Integration (VLSI) design becomes very complex due to the continuous integration of millions of gates in one chip based on Moore's law. Designers have encountered numerous report files during design iterations using timing and noise analysis tools. This paper presented our work using data mining techniques combined with HTML tables to extract and represent critical timing/noise data. When we apply this data-mining tool in real applications, the running speed is important. The software employs table look-up techniques in the programming for the reasonable running speed based on performance testing results. We added several advanced features for the application in one industry chip design.

Keywords : VLSI design, data mining, big data, HTML forms, web, VLSI, EDA, timing, noise
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