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Intelligent and Optimized Placement for CPLD Devices

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Abstract : The PLD/CPLD devices are widely used for logic synthesis since several decades. Based on sum of product terms (PTs) architecture, the PLD/CPLD offer a high degree of flexibility to support various application requirements. They are suitable for large combinational logic, finite state machines as well as intensive I/O designs. CPLDs offer very predictable timing characteristics and are therefore ideal for critical control applications. This paper describes how the logic synthesis techniques, such as 1) XOR detection, 2) logic doubling, 3) complement of a Boolean function are combined, applied and used to optimize the CPLDs devices architecture that is based on PAL-like macrocells. Our goal is to use these techniques for minimizing the number of macrocells required to implement a circuit and minimize the delay of mapped circuit.

Keywords : CPLD, doubling, optimization, XOR
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