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A Study on ESD Protection Circuit Applying Silicon Controlled Rectifier-Based Stack Technology with High Holding Voltage

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Abstract : In this study, an improved Electrostatic Discharge (ESD) protection circuit with low trigger voltage and high holding voltage is proposed. ESD has become a serious problem in the semiconductor process because the semiconductor density has become very high these days. Therefore, much research has been done to prevent ESD. The proposed circuit is a stacked structure of the new unit structure combined by the Zener Triggering (SCR ZTSCR) and the High Holding Voltage SCR (HHVSCR). The simulation results show that the proposed circuit has low trigger voltage and high holding voltage. And the stack technology is applied to adjust the various operating voltage. As the results, the holding voltage is 7.7 V for 2-stack and 10.7 V for 3-stack.

Keywords : ESD, SCR, latch-up, power clamp, holding voltage
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