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Designing and Simulation of a CMOS Square Root Analog Multiplier

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Abstract : A new CMOS low voltage current-mode four-quadrant analog multiplier based on the squarer circuit with voltage output is presented. The proposed circuit is composed of a pair of current subtractors, a pair differential-input V-I converters and a pair of voltage squarers. The circuit was simulated using HSPICE simulator in standard 0.18 µm CMOS level 49 MOSIS (BSIM3 V3.2 SPICE-based). Simulation results show the performance of the proposed circuit and experimental results are given to confirm the operation. This topology of multiplier results in a high-frequency capability with low power consumption. The multiplier operates for a power supply ±1.2V. The simulation results of analog multiplier demonstrate a THD of 0.65% in 10MHz, a −3dB bandwidth of 1.39GHz, and a maximum power consumption of 7.1mW.

Keywords : analog processing circuit, WTA, LTA, low voltage
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