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A CMOS-Integrated Hall Plate with High Sensitivity

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Abstract : An improved cross-shaped hall plate with high sensitivity is described in this paper. Among different geometries that have been simulated and measured using Helmholtz coil. The paper describes the physical hall plate design and implementation in a 0.18-µm CMOS technology. In this paper, the biasing is a constant voltage mode. In the voltage mode, magnetic field is converted into an output voltage. The output voltage is typically in the order of micro- to millivolt and therefore, it must be amplified before being transmitted to the outside world. The study, design and performance optimization of hall plate has been carried out with the COMSOL Multiphysics. It is used to estimate the voltage distribution in the hall plate with and without magnetic field and to optimize the geometry. The simulation uses the nominal bias current of 1mA. The applied magnetic field is in the range from 0 mT to 20 mT. Measured results of the one structure over the 10 available samples show for the best sensitivity of 2.5 %/T at 20mT.

Keywords : cross-shaped hall plate, sensitivity, CMOS technology, Helmholtz coil
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