

## Low Power, Highly Linear, Wideband LNA in Wireless SOC

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**Abstract :** In this paper a highly linear CMOS low noise amplifier (LNA) for ultra-wideband (UWB) applications is proposed. The proposed LNA uses a linearization technique to improve second and third-order intercept points (IIP3). The linearity is cured by repealing the common-mode section of all intermodulation components from the cascade topology current with optimization of biasing current use symmetrical and asymmetrical circuits for biasing. Simulation results show that maximum gain and noise figure are 6.9dB and 3.03-4.1dB over a 3.1-10.6 GHz, respectively. Power consumption of the LNA core and IIP3 are 2.64 mW and +4.9dBm respectively. The wideband input impedance matching of LNA is obtained by employing a degenerating inductor ( $|S_{11}| < -9.1$  dB). The circuit proposed UWB LNA is implemented using 0.18  $\mu$ m based CMOS technology.

**Keywords :** highly linear LNA, low-power LNA, optimal bias techniques

**Conference Title :** ICACSPS 2017 : International Conference on Analog Circuits and Signal Processing Systems

**Conference Location :** New York, United States

**Conference Dates :** August 07-08, 2017