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Study of Heat Conduction in Multicore Chips

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Abstract : A method of temperature calculations is developed to study the conditions leading to hot spot occurrence on multicore chips. A physical model which has salient features of multicore chips is incorporated for the analysis. The model consists of active and background cell laid out in a checkered pattern, and this pattern repeats itself in each fine grain active cells. The die has three layers i) body ii) buried oxide layer iii) wiring layer, stacked one above the other with heat source placed at the interface between wiring and buried oxide layer. With this model we propose analytical method to calculate the target hotspot temperature, heat flow to top and bottom layers of the die and thermal resistance components at each granularity level, assuming appropriate values of die dimensions and parameters. Finally we attempt to find an easier method for the calculation of the target hotspot temperature using graph.

Keywords : checkered pattern, granularity level, heat conduction, multicore chips, target hotspot temperature
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