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The Investigation of the Impact of Process and Location Parameters in Warpage Study of Semiconductor Packages

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Abstract : The primary advantage of package-on-package (PoP) packaging is that since it has less volume, it weighs less. But this is also related to its principal drawback, which is warpage. This research investigates how PoP package warpage patterns are affected by assembling process parameters, including substrate temperature, injection speed, injection temperature, and compound forces. We also investigate how warpage patterns are affected by the location of the silicon chip. The methodologies used in this research are design of experiment and warpage simulation via ANSYS. We propose a regression model to predict the warpage value as a function of substrate temperature, injection speed, injection temperature, and compound forces. Our results show that interaction effects exist between substrate temperature and compound forces and between injection speed and injection temperature. Therefore, determining the optimal values for substrate temperature, compound forces, injection speed, and injection temperature cannot be done individually. Also, our results show that the warpage patterns based on the location of silicon chips can be classified into 11 groups, with the largest warpage occurring at the left-most and right-most sides.

Keywords : package-on-package, warpage, design of experiment, simulation
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