World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:8, No:04, 2014

A New Full Adder Cell for High Performance Low Power Applications

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Abstract : In this paper, a new low-power high-performance full adder is presented based on a new design method. The proposed method relies on pass gate design and provides full-swing circuits with minimum number of transistors. The method has been applied on SUM, COUT and XOR-XNOR modules resulting on rail-to-rail intermediate and output signals with no feedback transistors. The presented full adder cell has been simulated in 45 and 32 nm CMOS technologies using HSPICE considering parasitic capacitance and compared to several well-known designs from literature. In addition, the proposed cell has been extensively evaluated with different output loads, supply voltages, temperatures, threshold voltages, and operating frequencies. Results show that it functions properly under all mentioned conditions and exhibits less PDP compared to other design styles.

Keywords : full adders, low-power, high-performance, VLSI design
Conference Title : ICECSE 2014 : International Conference on Electrical, Computer and Systems Engineering
Conference Location : Paris, France
Conference Dates : April 28-29, 2014