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Design and Simulation Interface Circuit for Piezoresistive Accelerometers with Offset Cancellation Ability

Authors : Mohsen Bagheri, Ahmad Afifi

Abstract : This paper presents a new method for read out of the piezoresistive accelerometer sensors. The circuit works based on instrumentation amplifier and it is useful for reducing offset in Wheatstone bridge. The obtained gain is 645 with 1 μv/°c equivalent drift and 1.58 mw power consumption. A Schmitt trigger and multiplexer circuit control output node. A high speed counter is designed in this work. The proposed circuit is designed and simulated in 0.18 μm CMOS technology with 1.8 v power supply.

Keywords : piezoresistive accelerometer, zero offset, Schmitt trigger, bidirectional reversible counter
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