World Academy of Science, Engineering and Technology
International Journal of Computer and Systems Engineering
Vol:11, No:03, 2017

Optimal Number and Placement of Vertical Links in 3D Network-On-Chip

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Abstract : 3D technology can lead to a significant reduction in power and average hop-count in Networks on Chip (NoCs). It offers short and fast vertical links which copes with the long wire problem in 2D NoCs. This work proposes heuristic-based method to optimize number and placement of vertical links to achieve specified performance goals. Experiments show that significant improvement can be achieved by using a specific number of vertical interconnect.

Keywords : interconnect optimization, monolithic inter-tier vias, network on chip, system on chip, through silicon vias, three dimensional integration circuits
Conference Title : ICPP 2017 : International Conference on Parallel Processing
Conference Location : Rome, Italy
Conference Dates : March 05-06, 2017