World Academy of Science, Engineering and Technology
International Journal of Mathematical and Computational Sciences
Vol:14, No:12, 2020

Analysis of Vertical Hall Effect Device Using Current-Mode

Authors : Kim Jin Sup

Abstract : This paper presents a vertical hall effect device using current-mode. Among different geometries that have been studied and simulated using COMSOL Multiphysics, optimized cross-shaped model displayed the best sensitivity. The cross-shaped model emerged as the optimum plate to fit the lowest noise and residual offset and the best sensitivity. The symmetrical cross-shaped hall plate is widely used because of its high sensitivity and immunity to alignment tolerances resulting from the fabrication process. The hall effect device has been designed using a 0.18-μm CMOS technology. The simulation uses the nominal bias current of 12μA. The applied magnetic field is from 0 mT to 20 mT. Simulation results achieved in COMSOL and validated with respect to the electrical behavior of equivalent circuit for Cadence. Simulation results of the one structure over the 13 available samples shows for the best geometry a current-mode sensitivity of 6.6 %/T at 20mT. Acknowledgment: This work was supported by Institute for Information & communications Technology Promotion (IITP) grant funded by the Korea government (MSIP) (No. R7117-16-0165, Development of Hall Effect Semiconductor for Smart Car and Device).

Keywords : vertical hall device, current-mode, crossed-shaped model, CMOS technology
Conference Title : ICSRD 2020 : International Conference on Scientific Research and Development
Conference Location : Chicago, United States
Conference Dates : December 12-13, 2020