

## High-Efficiency Comparator for Low-Power Application

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**Abstract :** In this paper, dynamic comparator structure employing two methods for power consumption reduction with applications in low-power high-speed analog-to-digital converters have been presented. The proposed comparator has low consumption thanks to power reduction methods. They have the ability for offset adjustment. The comparator consumes 14.3  $\mu$ W at 100 MHz which is equal to 11.8 fJ. The comparator has been designed and simulated in 180 nm CMOS. Layouts occupy 210  $\mu$ m<sup>2</sup>.

**Keywords :** efficiency, comparator, power, low

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