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A High Time Resolution Digital Pulse Width Modulator Based on Field Programmable Gate Array's Phase Locked Loop Megafunction

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Abstract : The digital pulse width modulator (DPWM) is the crucial building block for digitally-controlled DC-DC switching converter, which converts the digital duty ratio signal into its analog counterpart to control the power MOSFET transistors on or off. With the increase of switching frequency of digitally-controlled DC-DC converter, the DPWM with higher time resolution is required. In this paper, a 15-bits DPWM with three-level hybrid structure is presented; the first level is composed of a7-bits counter and a comparator, the second one is a 5-bits delay line, and the third one is a 3-bits digital dither. The presented DPWM is designed and implemented using the PLL megafunction of FPGA (Field Programmable Gate Arrays), and the required frequency of clock signal is 128 times of switching frequency. The simulation results show that, for the switching frequency of 2 MHz, a DPWM which has the time resolution of 15 ps is achieved using a maximum clock frequency of 256MHz. The designed DPWM in this paper is especially useful for high-frequency digitally-controlled DC-DC switching converters.

Keywords : DPWM, digitally-controlled DC-DC switching converter, FPGA, PLL megafunction, time resolution
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