

Power Integrity Analysis of Power Delivery System in High Speed Digital FPGA Board

Authors : Anil Kumar Pandey

Abstract : Power plane noise is the most significant source of signal integrity (SI) issues in a high-speed digital design. In this paper, power integrity (PI) analysis of multiple power planes in a power delivery system of a 12-layer high-speed FPGA board is presented. All 10 power planes of HSD board are analyzed separately by using 3D Electromagnetic based PI solver, then the transient simulation is performed on combined PI data of all planes along with voltage regulator modules (VRMs) and 70 current drawing chips to get the board level power noise coupling on different high-speed signals. De-coupling capacitors are placed between power planes and ground to reduce power noise coupling with signals.

Keywords : power integrity, power-aware signal integrity analysis, electromagnetic simulation, channel simulation

Conference Title : ICEPST 2016 : International Conference on Electronic Packaging, Systems, and Technology

Conference Location : Paris, France

Conference Dates : November 21-22, 2016