Area Efficient Carry Select Adder Using XOR Gate Design

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Abstract : The AOI (AND – OR- INVERTER) based design of XOR gate is proposed in this paper with less number of gates. This new XOR gate required four basic gates and basic gate include only AND, OR, Inverter (AOI). Conventional XOR gate required five basic gates. Ripple Carry Adder (RCA) used in parallel addition but propagation delay time is large. RCA replaced with Carry Select Adder (CSLA) to reduce propagation delay time. CSLA design with dual RCA considering carry = '0' and carry = '1', so it is not an area efficient adder. To make area efficient, modified CSLA is designed with single RCA considering carry = '0' and another RCA considering carry = '1' replaced with Binary to Excess 1 Converter (BEC). Now replacement of conventional XOR gate by new design of XOR gate in modified CSLA reduces much area compared to regular CSLA and modified CSLA.

Keywords : CSLA, BEC, XOR gate, area efficient