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A Fault-Tolerant Full Adder in Double Pass CMOS Transistor

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Abstract : This paper presents a fault-tolerant implementation for adder schemes using the dual duplication code. To prove the efficiency of the proposed method, the circuit is simulated in double pass transistor CMOS 32nm technology and some transient faults are voluntary injected in the Layout of the circuit. This fully differential implementation requires only 20 transistors which mean that the proposed design involves 28.57% saving in transistor count compared to standard CMOS technology.

Keywords : digital electronics, integrated circuits, full adder, 32nm CMOS tehnology, double pass transistor technology, fault toleance, self-checking
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