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Design and Implementation of 2D Mesh Network on Chip Using VHDL

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Abstract : Nowadays, using the advancement of technology in semiconductor device fabrication, many transistors can be integrated to a single chip (VLSI). Although the growth chip density potentially eases systems-on-chip (SoCs) integrating thousands of processing element (PE) such as memory, processor, interfaces cores, system complexity, high-performance interconnect and scalable on-chip communication architecture become most challenges for many digital and embedded system designers. Networks-on-chip (NoCs) becomes a new paradigm that makes possible integrating heterogeneous devices and allows many communication constraints and performances. In this paper, we are interested for good performance and low area for implementation and a behavioral modeling of network on chip mesh topology design using VHDL hardware description language with performance evaluation and FPGA implementation results.

Keywords : design, implementation, communication system, network on chip, VHDL
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