

## Optimization of SWL Algorithms Using Alternative Adder Module in FPGA

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**Abstract :** Recently single-bit ternary FIR-like filter (SBTFF) hardware synthesize in FPGA is reported and compared with multi-bit FIR filter on similar spectral characteristics. Results shows that SBTFF dominates upon multi-bit filter overall. In this paper, an optimized adder module for ternary quantized sigma-delta modulated signal is presented. The adder is simulated using ModelSim for functional verification the area-performance of the proposed adder were obtained through synthesis in Xilinx and compared to conventional adder trees. The synthesis results show that the proposed adder tree achieves higher clock rates and lower chip area at higher inputs to the adder block; whereas conventional adder tree achieves better performance and lower chip area at lower number of inputs to the same adder block. These results enhance the usefulness of existing short word length DSP algorithms for fast and efficient mobile communication.

**Keywords :** short word length (SWL), DSP algorithms, FPGA, SBTFF, VHDL

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