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Optimizing Power in Sequential Circuits by Reducing Leakage Current Using Enhanced Multi Threshold CMOS

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Abstract : The demand for portability, performance and high functional integration density of digital devices leads to the scaling of complementary metal oxide semiconductor (CMOS) devices inevitable. The increase in power consumption, coupled with the increasing demand for portable/hand-held electronics, has made power consumption a dominant concern in the design of VLSI circuits today. MTCMOS technology provides low leakage and high performance operation by utilizing high speed, low Vt (LVT) transistors for logic cells and low leakage, high Vt (HVT) devices as sleep transistors. Sleep transistors disconnect logic cells from the supply and/or ground to reduce the leakage in the sleep mode. In this technology, energy consumption while doing the mode transition and minimum time required to turn ON the circuit upon receiving the wake up signal are issues to be considered because these can adversely impact the performance of VLSI circuit. In this paper we are introducing an enhancing method of MTCMOS technology to optimize the power in MTCMOS sequential circuits.

Keywords : power consumption, ultra-low power, leakage, sub threshold, MTCMOS
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