World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:9, No:08, 2015

A Low-Power, Low-Noise and High-Gain 58~66 GHz CMOS Receiver Front-End for Short-Range High-Speed Wireless Communications

Authors : Yo-Sheng Lin, Jen-How Lee, Chien-Chin Wang

Abstract : A 60-GHz receiver front-end using standard 90-nm CMOS technology is reported. The receiver front-end comprises a wideband low-noise amplifier (LNA), and a double-balanced Gilbert cell mixer with a current-reused RF single-to-differential (STD) converter, an LO Marchand balun and a baseband amplifier. The receiver front-end consumes 34.4 mW and achieves LO-RF isolation of 60.7 dB, LO-IF isolation of 45.3 dB and RF-IF isolation of 41.9 dB at RF of 60 GHz and LO of 59.9 GHz. At IF of 0.1 GHz, the receiver front-end achieves maximum conversion gain (CG) of 26.1 dB at RF of 64 GHz and CG of 25.2 dB at RF of 60 GHz. The corresponding 3-dB bandwidth of RF is 7.3 GHz (58.4 GHz to 65.7 GHz). The measured minimum noise figure was 5.6 dB at 64 GHz, one of the best results ever reported for a 60 GHz CMOS receiver front-end. In addition, the measured input 1-dB compression point and input third-order inter-modulation point are -33.1 dBm and -23.3 dBm, respectively, at 60 GHz. These results demonstrate the proposed receiver front-end architecture is very promising for 60 GHz direct-conversion transceiver applications.

Keywords : CMOS, 60 GHz, direct-conversion transceiver, LNA, down-conversion mixer, marchand balun, current-reused
Conference Title : ICIAE 2015 : International Conference on Industrial and Applied Electronics
Conference Location : Venice, Italy
Conference Dates : August 13-14, 2015