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Design of Speedy, Scanty Adder for Lossy Application Using QCA

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Abstract : Recent trends in microelectronics technology have gradually changed the strategies used in very large scale integration (VLSI) circuits. Complementary Metal Oxide Semiconductor (CMOS) technology has been the industry standard for implementing VLSI device for the past two decades, but due to scale-down issues of ultra-low dimension achievement is not achieved so far. Hence it paved a way for Quantum Cellular Automata (QCA). It is only one of the many alternative technologies proposed as a replacement solution to the fundamental limit problem that CMOS technology will impose in the years to come. In this brief, presented a new adder that possesses high speed of operation occupying less area is proposed. This adder is designed especially for error tolerant application. Hence in the proposed adder, the overall area (cell count) and simulation time are reduced by 88 and 73 percent respectively. Various results of the proposed adder are shown and described.

Keywords : quantum cellular automata, carry look ahead adder, ripple carry adder, lossy application, majority gate, crossover
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