

## I<sup>2</sup>C Master-Slave Integration

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**Abstract :** This paper describes I<sup>2</sup>C Slave implementation using I<sup>2</sup>C master obtained from the OpenCores website. This website provides free Verilog and VHDL Codes to users. The design implementation for the I<sup>2</sup>C slave is in Verilog Language and uses EDA tools for ASIC design known as ModelSim from Mentor Graphic. This tool is used for simulation and verification purposes. Common application for this I<sup>2</sup>C Master-Slave integration is also included. This paper also addresses the advantages and limitations of the said design.

**Keywords :** I<sup>2</sup>C, master, OpenCores, slave, Verilog, verification

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