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Performance Improvement of SOI-Tri Gate FinFET Transistor Using High-K Dielectric with Metal Gate

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Abstract : SOI TRI GATE FinFET transistors have emerged as novel devices due to its simple architecture and better performance: better control over short channel effects (SCEs) and reduced power dissipation due to reduced gate leakage currents. As the oxide thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the SiO2 gate oxide with a high-κ material allows increased gate capacitance without the associated leakage effects. In this paper, SOI TRI-GATE FinFET structure with use of high K dielectric materials (HfO2) and SiO2 dielectric are simulated using the 3-D device simulator Devedit and Atlas of TCAD Silvaco. The simulated results exhibits significant improvements in the performances of SOI TRI GATE FinFET with gate oxide HfO2 compared with conventional gate oxide SiO2 for the same structure. SOI TRI-GATE FinFET structure with the use of high K materials (HfO2) in gate oxide results into the increase in saturation current, threshold voltage, on-state current and Ion/Ioff ratio while off-state current, subthreshold slope and DIBL effect are decreased.

Keywords : technology SOI, short-channel effects (SCEs), multi-gate SOI MOSFET, SOI-TRI Gate FinFET, high-K dielectric, Silvaco software
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