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Designing Equivalent Model of Floating Gate Transistor

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Abstract : In this paper, an equivalent model for floating gate transistor has been proposed. Using the floating gate voltage value, capacitive coupling coefficients has been found at different bias conditions. The amount of charge present on the gate has been then calculated using the transient models of hot electron programming and Fowler-Nordheim Tunnelling. The proposed model can be extended to the transient conditions as well. The SPICE equivalent model is designed and current-voltage characteristics and Transfer characteristics are comparatively analysed. The dc current-voltage characteristics, as well as dc transfer characteristics, have been plotted for an FGMOS with W/L=0.25μm/0.375μm, the inter-poly capacitance of 0.8fF for both programmed and erased states. The Comparative analysis has been made between the present model and capacitive coefficient coupling methods which were already available.

Keywords : FGMOS, floating gate transistor, capacitive coupling coefficient, SPICE model
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