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Practical Simulation Model of Floating-Gate MOS Transistor in Sub 100 nm Technologies

Authors : Zina Saheb, Ezz El-Masry

Abstract : As CMOS technology scaling down, Silicon oxide thickness (SiO2) become very thin (few Nano meters). When SiO2 is less than 3nm, gate direct tunneling (DT) leakage current becomes a dormant problem that impacts the transistor performance. Floating gate MOSFET (FGMOSFET) has been used in many low-voltage and low-power applications. Most of the available simulation models of FGMOSFET for analog circuit design does not account for gate DT current and there is no accurate analysis for the gate DT. It is a crucial to use an accurate mode in order to get a realistic simulation result that account for that DT impact on FGMOSFET performance effectively.

Keywords : CMOS transistor, direct-tunneling current, floating-gate, gate-leakage current, simulation model
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