World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:9, No:04, 2015

Design Of High Sensitivity Transceiver for WSN

Authors : A. Anitha, M. Aishwariya

Abstract : The realization of truly ubiquitous wireless sensor networks (WSN) demands Ultra-low power wireless communication capability. Because the radio transceiver in a wireless sensor node consumes more power when compared to the computation part it is necessary to reduce the power consumption. Hence, a low power transceiver is designed and implemented in a 120 nm CMOS technology for wireless sensor nodes. The power consumption of the transceiver is reduced still by maintaining the sensitivity. The transceiver designed combines the blocks including differential oscillator, mixer, envelope detector, power amplifiers, and LNA. RF signal modulation and demodulation is carried by On-Off keying method at 2.4 GHz which is said as ISM band. The transmitter demonstrates an output power of 2.075 mW while consuming a supply voltage of range 1.2 V-5.0 V. Here the comparison of LNA and power amplifier is done to obtain an amplifier which produces a high gain of 1.608 dB at receiver which is suitable to produce a desired sensitivity. The multistage RF amplifier is used to improve the gain at the receiver side. The power dissipation of the circuit is in the range of 0.183-0.323 mW. The receiver achieves a sensitivity of about -95 dBm with data rate of 1 Mbps.

Keywords : CMOS, envelope detector, ISM band, LNA, low power electronics, PA, wireless transceiver
Conference Title : ICCNMC 2015 : International Conference on Communications, Networking and Mobile Computing
Conference Location : London, United Kingdom
Conference Dates : April 24-25, 2015