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Design of Low Power FSK Receiver

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Abstract : This letter presents a novel frequency-shift keying(FSK) receiver using PLL-based FSK demodulator, thereby achieving high sensitivity and low power consumption. The proposed receiver comprises a power amplifier, mixer, 3-stage ring oscillator, PLL based demodulator. Moreover, the proposed receiver is fabricated using 0.12µm CMOS process and consumes 0.7Mw. Measurement results demonstrate that the proposed receiver has a sensitivity of -93dbm with 1Mbps data rate in receiving a 2.4 GHz FSK signal.

Keywords : CMOS FSK receiver, phase locked loop (PLL), 3-stage ring oscillator, FSK signal
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