World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:9, No:10, 2015

Physical Verification Flow on Multiple Foundries

Authors : Rohaya Abdul Wahab, Raja Mohd Fuad Tengku Aziz, Nazaliza Othman, Sharifah Saleh, Nabihah Razali, Muhammad Al Baqir Zinal Abidin, Md Hanif Md Nasir

Abstract : This paper will discuss how we optimize our physical verification flow in our IC Design Department having various rule decks from multiple foundries. Our ultimate goal is to achieve faster time to tape-out and avoid schedule delay. Currently the physical verification runtimes and memory usage have drastically increased with the increasing number of design rules, design complexity and the size of the chips to be verified. To manage design violations, we use a number of solutions to reduce the amount of violations needed to be checked by physical verification engineers. The most important functions in physical verifications are DRC (design rule check), LVS (layout vs. schematic) and XRC (extraction). Since we have a multiple number of foundries for our design tape-outs, we need a flow that improve the overall turnaround time and ease of use of the physical verification process. The demand for fast turnaround time is even more critical since the physical design is the last stage before sending the layout to the foundries.

Keywords : physical verification, DRC, LVS, XRC, flow, foundry, runset
Conference Title : ICECECE 2015 : International Conference on Electrical, Computer, Electronics and Communication Engineering
Conference Location : Osaka, Japan
Conference Dates : October 08-09, 2015