

Design of a High Performance T/R Switch for 2.4 GHz RF Wireless Transceiver in 0.13 μm CMOS Technology

Authors : Mohammad Arif Sobhan Bhuiyan, Mamun Bin Ibne Reaz

Abstract : The rapid advancement of CMOS technology, in the recent years, has led the scientists to fabricate wireless transceivers fully on-chip which results in smaller size and lower cost wireless communication devices with acceptable performance characteristics. Moreover, the performance of the wireless transceivers rigorously depends on the performance of its first block T/R switch. This article proposes a design of a high performance T/R switch for 2.4 GHz RF wireless transceivers in 0.13 μm CMOS technology. The switch exhibits 1- dB insertion loss, 37.2-dB isolation in transmit mode and 1.4-dB insertion loss, 25.6-dB isolation in receive mode. The switch has a power handling capacity (P1dB) of 30.9-dBm. Besides, by avoiding bulky inductors and capacitors, the size of the switch is drastically reduced and it occupies only (0.00296) mm² which is the lowest ever reported in this frequency band. Therefore, simplicity and low chip area of the circuit will trim down the cost of fabrication as well as the whole transceiver.

Keywords : CMOS, ISM band, SPDT, t/r switch, transceiver

Conference Title : ICIEE 2015 : International Conference on Informatics and Electronics Engineering

Conference Location : San Francisco, United States

Conference Dates : June 07-08, 2015