

Implementation of Iterative Algorithm for Earthquake Location

Authors : Hussain K. Chaiel

Abstract : The development in the field of the digital signal processing (DSP) and the microelectronics technology reduces the complexity of the iterative algorithms that need large number of arithmetic operations. Virtex-Field Programmable Gate Arrays (FPGAs) are programmable silicon foundations which offer an important solution for addressing the needs of high performance DSP designer. In this work, Virtex-7 FPGA technology is used to implement an iterative algorithm to estimate the earthquake location. Simulation results show that an implementation based on block RAMB36E1 and DSP48E1 slices of Virtex-7 type reduces the number of cycles of the clock frequency. This enables the algorithm to be used for earthquake prediction.

Keywords : DSP, earthquake, FPGA, iterative algorithm

Conference Title : ICCSEE 2015 : International Conference on Civil, Structural and Earthquake Engineering

Conference Location : Toronto, Canada

Conference Dates : June 15-16, 2015