

Design of CMOS CFOA Based on Pseudo Operational Transconductance Amplifier

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Abstract : A novel design technique employing CMOS Current Feedback Operational Amplifier (CFOA) is presented. The feature of consumption which has a very low power in designing pseudo-OTA is used to decreasing the total power consumption of the proposed CFOA. This design approach applies pseudo-OTA as input stage cascaded with buffer stage. Moreover, the DC input offset voltage and harmonic distortion (HD) of the proposed CFOA are very low values compared with the conventional CMOS CFOA due to symmetrical input stage. P-Spice simulation results using 0.18 μm MIETEC CMOS process parameters using supply voltage of $\pm 1.2\text{V}$ and 50 μA biasing current. The P-Spice simulation shows excellent improvement of the proposed CFOA over existing CMOS CFOA. Some of these performance parameters, for example, are DC gain of 62. dB, open-loop gain-bandwidth product of 108 MHz, slew rate (SR+) of +71.2V/ μS , THD of -63dB and DC consumption power (PC) of 2mW.

Keywords : pseudo-OTA used CMOS CFOA, low power CFOA, high-performance CFOA, novel CFOA

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