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Design and Study of a Low Power High Speed 8 Transistor Based Full Adder Using Multiplexer and XOR Gates

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Abstract : In this paper, we propose a new technique for implementing a low power high speed full adder using 8 transistors. Full adder circuits are used comprehensively in Application Specific Integrated Circuits (ASICs). Thus it is desirable to have high speed operation for the sub components. The explored method of implementation achieves a high speed low power design for the full adder. Simulated results indicate the superior performance of the proposed technique over conventional 28 transistor CMOS full adder. Detailed comparison of simulated results for the conventional and present method of implementation is presented.

Keywords : high speed low power full adder, 2-T MUX, 3-T XOR, 8-T FA, pass transistor logic, CMOS (complementary metal oxide semiconductor)
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