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Design and Study of a Low Power High Speed Full Adder Using GDI Multiplexer

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Abstract : In this paper, we propose a new technique for implementing a low power full adder using a set of GDI multiplexers. Full adder circuits are used comprehensively in Application Specific Integrated Circuits (ASICs). Thus it is desirable to have low power operation for the sub components. The explored method of implementation achieves a low power design for the full adder. Simulated results using state-of-art Tanner tool indicates the superior performance of the proposed technique over conventional CMOS full adder. Detailed comparison of simulated results for the conventional and present method of implementation is presented.

Keywords : low power full adder, 2-T GDI MUX, ASIC (application specific integrated circuit), 12-T FA, CMOS (complementary metal oxide semiconductor)
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