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Functional and Stimuli Implementation and Verification of Programmable Peripheral Interface (PPI) Protocol

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Abstract : We present the stimuli implementation and verification of a Programmable Peripheral Interface (PPI) 8255. It involves a designing and verification of configurable intellectual property (IP) module of PPI protocol using Verilog HDL for implementation part and System Verilog for verification. The overview of the PPI-8255 presented then the design specification implemented for the work following the functional description and pin configuration of PPI-8255. The coverage report of design shows that our design and verification environment covered 100% functionality in accordance with the design specification generated by the Questa Sim 10.0b.

Keywords : Programmable Peripheral Interface (PPI), verilog HDL, system verilog, questa sim
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