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An Adder with Novel PMOS and NMOS for Ultra Low Power Applications in Deep Submicron Technology

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Abstract : Power has became a burning issue in modern VLSI design. As the technology advances especially below 45nm, technology of leakage power became a big problem apart of the dynamic power. This paper presents a full adder with novel PMOS and NMOS which consume less power compare to conventional full adder, DTMOS full adder. This paper shows different types of adders and their power consumption, area, and delay. All the experiments have been carried out using Cadence® Virtuoso® design lay out editor which shows power consumption of different types of adders.

Keywords : average power, leakage power, delay, DTMOS, PDP
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