Optimization of Reliability Test Plans: Increase Wafer Fabrication Equipments Uptime

Authors : Swajeeth Panchangam, Arun Rajendran, Swarnim Gupta, Ahmed Zeouita

Abstract : Semiconductor processing chambers tend to operate in controlled but aggressive operating conditions (chemistry, plasma, high temperature etc.) Owing to this, the design of this equipment requires developing robust and reliable hardware and software. Any equipment downtime due to reliability issues can have cost implications both for customers in terms of tool downtime (reduced throughput) and for equipment manufacturers in terms of high warranty costs and customer trust deficit. A thorough reliability assessment of critical parts and a plan for preventive maintenance/replacement schedules need to be done before tool shipment. This helps to save significant warranty costs and tool downtimes in the field. However, designing a proper reliability test plan to accurately demonstrate reliability targets with proper sample size and test duration is quite challenging. This is mainly because components can fail in different failure modes that fit into different Weibull beta value distributions. Without apriori Weibull beta of a failure mode under consideration, it always leads to over/under utilization of resources, which eventually end up in false positives or false negatives estimates. This paper proposes a methodology to design a reliability test plan with optimal model size/duration/both (independent of apriori Weibull beta). This methodology can be used in demonstration tests and can be extended to accelerated life tests to further decrease sample size/test duration.

Keywords : reliability, stochastics, preventive maintenance
Conference Title : ICMSE 2025 : International Conference on Mechanical and Systems Engineering
Conference Location : Bengaluru, India
Conference Dates : January 30-31, 2025

Open Science Index, Mechanical and Industrial Engineering Vol:19, No:01, 2025 publications.waset.org/abstracts/192542.pdf