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On Chip Transmission Line Models in 65nm CMOS Technology with Multilevel Metallization Process

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Abstract : In this paper, two on-chip compact transmission lines (TLs) based on the coplanar waveguide (CPW) and microstrip designs are proposed for the 65nm Complementary Metal-Oxide-Semiconductor (CMOS) technology with multilevel metallization process. These transmission lines are analysed using High-Frequency Structure Simulator (HFSS) and 3D electromagnetic full wave simulator. The performance of the transmission line is improved using air gap-based structures within the constraints of fabrication techniques. Through this work it is established that for the 65 nm CMOS technology process, both TL models give a comparable insertion loss performance of < 1.58 dB/mm over the band of 80GHz. However, it is found when matched for a characteristic impedance of 50Ω, the coplanar waveguide-based TL gives a reflection coefficient of about -30dB and the microstrip line-based TL gives only about -16dB over the 80GHz band. This work also brings out that at low frequency, both the TLs can be used where the reflection coefficient is < -25dB but at high frequency, the coplanar waveguide based TLs are the best suited with small penalty of increased area.

Keywords : coplanar waveguide, microstrip line, monolithic microwave integrated circuit, multilevel metallization process, characteristic impedance
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