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Spartan 6 - XC6SLX9 FPGA Implementation of Analog Waveforms Generator by Direct Digital Synthesis (DDS)

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Abstract : In the last thirty years, low-power Field Programmable Gate Arrays (FPGAs) have become more commonly used to implement countless applications in different electronics industry domains. Due to their flexible design, strong compatibility, parallel computing, and compared to the CPU architecture, FPGA accentuates computing efficiency and is considered one of the devices with the lowest application risk and the shortest development cycle among the variety of available programmable circuit families. This paper presents an experimental FPGA implementation of precise analog waveform generation using the Direct Digital Synthesis (DDS) method based on LookUp Table (LUT) by VHDL dataflow language-based ROM designed using embedded RAM of a Xilinx AMD SPARTAN 6 XC6SLX9/CSG324 FPGA Development Board. To provide ROM addresses for reading the stored sample values from the LUT, we use a VHDL-based counter, and these sample values are converted into a continuous analog waveform using a Digital Analog Converter (DAC). To integrate VHDL code into our FPGA chip, we use Vivado Design Suite, which is software for the synthesis and analysis of VHDL designs, and we will visualize the waveform using Vivado test bench, which is a proper VHDL source file used to drive simulations.

Keywords : SPARTAN 6, XC6SLX9, FPGA, VHDL
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