World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:9, No:01, 2015

Area-Efficient FPGA Implementation of an FFT Processor by Reusing Butterfly Units

Authors : Atin Mukherjee, Amitabha Sinha, Debesh Choudhury

Abstract : Fast Fourier transform (FFT) of large-number of samples requires larger hardware resources of field programmable gate arrays and it asks for more area as well as power. In this paper, an area efficient architecture of FFT processor is proposed, that reuses the butterfly units more than once. The FFT processor is emulated and the results are validated on Virtex-6 FPGA. The proposed architecture outperforms the conventional architecture of a N-point FFT processor in terms of area which is reduced by a factor of log_N(2) with the negligible increase of processing time.

Keywords : FFT, FPGA, resource optimization, butterfly units
Conference Title : ICSIP 2015 : International Conference on Signal and Image Processing
Conference Location : Singapore, Singapore
Conference Dates : January 08-09, 2015