World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:8, No:11, 2014

Horizontal-Vertical and Enhanced-Unicast Interconnect Testing Techniques for Network-on-Chip

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Abstract : One of the most important and challenging tasks in testing network-on-chip based system-on-chips (NoC based SoCs) is to verify the communication entity. It is important because of its usage for transferring both data packets and test patterns for intellectual properties (IPs) during normal and test mode. Hence, ensuring of NoC reliability is required for reliable IPs functionality and testing. On the other hand, it is challenging due to the required time to test it and the way of transferring test patterns from the tester to the NoC components. In this paper, two testing techniques for mesh-based NoC interconnections are proposed. The first one is based on one-by-one testing and the second one divides NoC interconnects into three parts, horizontal links of switches in even columns, horizontal links of switches in odd columns and all vertical. A design for testability (DFT) architecture is represented to send test patterns directly to each switch under test and also support the proposed testing techniques by providing a loopback path in each switch. The simulation results shows the second proposed testing mechanism outperforms in terms of test time because this method test all the interconnects in only three phases, independent to the number of existed interconnects in the network, while test time of other methods are highly dependent to the number of switches and interconnects in the NoC.

Keywords : on chip, interconnection testing, horizontal-vertical testing, enhanced unicast
Conference Title : ICCSCC 2014 : International Conference on Circuits, Systems, Computers and Communications
Conference Location : Venice, Italy
Conference Dates : November 13-14, 2014